NB4L52

2.5 to 5.5 V ECL D Flip-flop w/Differential Reset & Input Termination

Product Overview

For complete documentation, see the data sheet.

The NB4L52 is a differential Data and Clock D flipflop with a differential asynchronous Reset. The differential inputs incorporate internal 50-ohm termination resistors and will accept LVPECL, LVCMOS, LVTTL, CML, or LVDS logic levels. When Clock transitions from Low to High, Data will be transferred to the differential LVPECL outputs. The differential Clock inputs allow the NB4L52 to also be used as a negative edge triggered device. The device is housed in a small 3mm x 3mm 16 pin QFN package.

Features

- Maximum Input Clock Frequency > 4 GHz Typical
- 330 ps Typical Propagation Delay
- 145 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 750 mV PeaktoPeak, Typical
- Operating Range: VCC = 2.375 V to 5.5 V with VEE = 0 V

Applications

- High Performance Logic for ATE and Networking

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Bits	Input Level	Output Level	V_{CC} Typ (V)	t_{jitter} Typ (ps)	t_{pd} Typ (ns)	t_{su} Min (ns)	t_h Min (ns)	t_{rec} Typ (ns)	t_R & t_F Max (ps)	f_{Toggle} Typ (MHz)	Package Type
NB4L52MNG	5	Pb H	Active	D-Type	1		ECL		1	0.4	0.1	0.05	0.4	190	4000	QFN-16
NB4L52MNR2G	5	Pb H	Active	D-Type	1		ECL		1	0.4	0.1	0.05	0.4	190	4000	QFN-16