NB4N121K

Clock Fanout Buffer, 1:21 Differential, 3.3 V, with HCSL Level Output

Product Overview

For complete documentation, see the data sheet.

The NB4N121K is a Clock differential input fanout distribution 1 to 21 HCSL level differential outputs, optimized for ultra low propagation delay variation. The NB4N121K is designed with HCSL clock distribution for FBDIMM applications in mind. Inputs can accept differential LVPECL, CML, or LVDS levels. Single-ended LVPECL, CML, LVCMOS or LVTTL levels are accepted with the proper VREFAC supply (see Figures 5, 10, 11, 12, and 13). Clock input pins incorporate an internal 50 ohm on die termination resistors.

Features

- Typical Input Clock Frequency 100, 133, 166, 200, 266, 333 and400 MHz
- <1 ps RMS Additive Clock jitter
- Operating Range: VCC = 3.0 V to 3.6 V with VEE = 0 V
- 340 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay tPD 100 ps Maximum Propagation
- Delta tPD 100 ps Maximum Propagation Delay Variation Per Each Differential Pair
- Differential HCSL Output Level (700 mV Peak-to-Peak)

Benefits

- Meets wide range of FBDIMM bus frequencies
- Best in class for jitter performance
- Ensures operation in the majority of designs

Applications

- FBDIMM Clock Distribution
- PCIe I, II, II
- Networking
- Clock Distribution
- High End Computing

End Products

- FBDIMM Memory Support
- Servers
- Routers

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NB4N121KMNR2G	4.6	Pb H	Active	Buffer	1	1:21		HCSL	3.3	1	50	0.8	700	200		QFN-52