

NB4N111K

Clock Fanout Buffer, 1:10 Differential, 3.3 V, with HCSL Level Output

Product Overview

For complete documentation, see the data sheet.

The NB4N111K is a differential input clock 1 to 10 HCSL fanout buffer, optimized for ultra low propagation delay variation. The NB4N111K is designed with HCSL clock distribution for FBDIMM applications in mind. Inputs can accept differential LVPECL, CML, or LVDS levels. Single-ended LVPECL, CML, LVCMOS or LVTTTL levels are accepted with the proper VREFAC supply (see Figures 5, 10, 11, 12, and 13). Clock input pins incorporate an internal 50 ohm on die termination resistors.

Features

- Typical Input Clock Frequencies: 100, 133, 166, 200, 266, 333, and 400 MHz
- <1 ps RMS Additive Clock jitter
- Operating Range: VCC = 3.0 V to 3.6 V with VEE = 0 V
- 340 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay
- delta tpd 100 ps Maximum Propagation Delay Variation Per Each Differential Pair
- Differential HCSL Output Level

Benefits

- Meets wide range of FBDIMM bus frequencies
- Best in class for jitter performance
- Ensures operation in the majority of designs

Applications

- HCSL FBDIMM Memory CLOCK buffer
- General High Performance HCSL Fanout buffer
- Clock Distribution
- PCIe I, II, III
- Networking

End Products

- Servers
- Routers
- FBDIMM Memory Card

Part Electrical Specifications

Product	Pricing (\$/Unit)	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V _{CC} Typ (V)	t _{jitter} RMS Typ (ps)	t _{skew(o-o)} Max (ps)	t _{pd} Typ (ns)	t _R & t _F Max (ps)	f _{max} lock Typ (MHz)	f _{max} data Typ (Mbps)	Package Type
NB4N111KMNG	5.8053		Active	Buffer	1	1:10		HCSL	3.3	1	100	0.8	700	400		QFN-32
NB4N111KMNR4G	5.8053		Active	Buffer	1	1:10		HCSL	3.3	1	100	0.8	700	400		QFN-32