NB3W1200L

3.3 V 100/133 MHz Differential 1:12 Push-Pull Clock ZDB/Fanout Buffer for PCIe

Product Overview

For complete documentation, see the data sheet.

The NB3N1200K and NB3W1200L differential clock buffers are DB1200Z and DB1200ZL compliant and are designed to work in conjunction with a PCIe compliant source clock synthesizer to provide point-to-point clocks to multiple agents. The device is capable of distributing the reference clocks for Intel® QuickPath Interconnect (Intel QPI & UPI), PCIe Gen1/Gen2/Gen3/Gen4, SAS, SATA, and Intel Scalable Memory Interconnect (Intel SMI) applications. The VCO of the device is optimized to support 100 MHz and 133 MHz frequency operation. The NB3N1200K and NB3W1200L utilize pseudo-external feedback topology to achieve low input-to output delay variation. The NB3N1200K is configured with the HCSL buffer type, while the NB3W1200L is configured with the low-power NMOS Push-Pull buffer type.

Features

- 12 Differential Clock Output Pairs @ 0.7 V
- Low-Power NMOS Push-Pull Compatible Outputs for NB3W1200L
- Optimized 100 MHz and 133 MHz Operating Frequencies to Meet The Next Generation PCIe Gen 2/Gen 3/ Gen 4 and Intel QPI & UPI Phase Jitter
- DB1200ZL Compliant
- 3.3 V ±5% Supply Voltage Operation
- Fixed-Feedback for Lowest Input-To-Output Delay Variation
- SMBus Programmable Configurations to Allow Multiple Buffers in a Single Control Network
- PLL Bypass Configurable for PLL or Fanout Operation
- Programmable PLL Bandwidth
- 2 Tri-level Addresses Selection (9 SMBUS Addresses)

  For more features, see the data sheet

Applications

- Industrial
- Networking
- Computing
- Consumer

End Products

- Desktop
- Notebook
- Switchers/Routers
- Servers
- Set Top Box

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Channels	Input / Output Ratio	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} RMS Typ (ps)	$t_{skew(o-o)}$ Max (ps)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	f_{max} Clock Typ (MHz)	f_{max} Data Typ (Mbps)	Package Type
NB3W1200LMNTXG	3.25	Pb H	Active	Buffer	1	1:12	HCSL	HCSL	3.3		50	0	87.5			QFN-64