Product Overview

NB7V33M: Clock Divider, ÷4, 10 GHz, 1.8 V / 2.5 V, with CML Outputs

For complete documentation, see the data sheet.

The NB7V33M is a differential divide by 4 Clock divider with asynchronous reset. The differential Clock inputs incorporate internal 50-ohm termination resistors and will accept LVPECL, CML and LVDS logic levels. The NB7V33M produces a div 4 output copy of an input Clock operating up to 10GHz with minimal jitter. The Reset pin is asserted on the rising edge. Upon powerup, the internal flip-flops will attain a random state. The Reset allows for the synchronization of multiple NB7V33Ms in a system. The 16mA differential CML output provides matching internal 50-ohm termination which provides 400mV output swing when externally receiver terminated with 50-ohm to VCC. The NB7V33M is the div 4 version of the NB7V32M (div 2) and is offered in a low profile 3mm x 3mm 16-pin QFN package. The NB7V33M is a member of the GigaComm family of high performance clock products.

Features

- Maximum Input Clock Frequency > 10 GHz, typical
- 260 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV peaktopeak, typical
- Internal 50-ohm Input Termination Resistors
- Random Clock Jitter < 0.8 ps RMS
- 40C to +85C Ambient Operating Temperature

Applications

- Clock Divider

End Products

- ATE, Instrumentation

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Input Level	Output Level	V_{CC} Typ (V)	f_{Max} Typ (MHz)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	Package Type
NB7V33MMNG	6.49	Pb-free Halide free non AEC-Q and PPAP	Active	Divider	CML ECL LVDS	CML	1.8 2.5	11000	0.2	60	QFN-16
NB7V33MMNHTBG	6.49	Pb-free Halide free non AEC-Q and PPAP	Active	Divider	CML ECL LVDS	CML	1.8 2.5	11000	0.2	60	QFN-16
NB7V33MMNTXG	6.49	Pb-free Halide free non AEC-Q and PPAP	Active	Divider	CML ECL LVDS	CML	1.8 2.5	11000	0.2	60	QFN-16

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