Product Overview

MC14015B: Dual 4-Bit Static Shift Register

For complete documentation, see the data sheet.

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design - Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive goingedge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pb-Free Packages are Available*

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Channels	V_{CC} Min (V)	V_{CC} Max (V)	t_{pd} Max (ns)	I_O Max (mA)	Package Type
MC14015BDG	0.2541	Pb-free Halide free non AEC-Q and PPAP	Active	Shift Register	2	3	18	250	2.25	SOIC-16
MC14015BDR2G	0.18	Pb-free Halide free non AEC-Q and PPAP	Active	Shift Register	2	3	18	250	2.25	SOIC-16
NLV14015BDR2G	0.308	AEC Qualified PPAP Capable Pb-free Halide free	Active	Shift Register	2	3	18	250	2.25	SOIC-16

For more information please contact your local sales support at www.onsemi.com.

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