Product Overview

NB3N1900K: 3.3 V 100/133 MHz Differential 1:19 HCSL Clock ZDB/Fanout Buffer for PCIe

For complete documentation, see the data sheet.

The NB3N1900K differential clock buffers are designed to work in conjunction with a PCIe compliant source clock synthesizer to provide point-to-point clocks to multiple agents. The device is capable of distributing the reference clocks for Intel® QuickPath Interconnect (Intel QPI & UPI), PCIe Gen1, Gen2, Gen3, Gen4. The NB3N1900K internal PLL is optimized to support 100 MHz and 133 MHz frequency operation. The NB3N1900K supports HCSL output levels.

Features

- Fixed Feedback Path for Lowest Input-to-Output Delay
- Eight Dedicated OE# Pins for Hardware Control of Outputs
- PLL Bypass Configurable for PLL or Fanout Operation
- Selectable PLL Bandwidth
- Spread Spectrum Compatible: Tracks Input Clock Spreading for Low EMI
- SMBus Programmable Configurations
- 100 MHz and 133 MHz PLL Mode to Meet the Next Generation PCIe Gen2 / Gen 3 /Gen 4 and Intel QPI & UPI Phase Jitter
- 2 Tri-Level Addresses Selection (Nine SMBUS Addresses)
- Cycle-to-Cycle Jitter: < 50 ps
- Output-to-Output Skew: < 65 ps

For more features, see the data sheet

Applications

- Industrial
- Networking
- Computing
- Consumer
- PCIe Gen 1, Gen 2, Gen 3, Gen 4

End Products

- Desktop
- Notebook
- Switchers/Routers
- Servers
- Set Top Box

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Input Level	Output Level	Outputs Per Channel	V_{DD} Typ (V)	$t_{skew(O-O)}$ Max (ps)	F Max (MHz)	t_{jitter} Max (ps)	Package Type
NB3N1900KMNG		Pb-free Halide free	Active	HCSL	HCSL	19	3.3	85	133.33	50	QFN-72
NB3N1900KMNTWG		Pb-free Halide free	Active	HCSL	HCSL	19	3.3	85	133.33	50	QFN-72
NB3N1900KMNTXG		Pb-free Halide free	Active	HCSL	HCSL	19	3.3	85	133.33	50	QFN-72

For more information please contact your local sales support at www.onsemi.com.

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