

## Product Overview

### MC100EP196: 3.3 V ECL Programmable Delay Chip

For complete documentation, see the data sheet.



The MC100EP196 is a programmable delay chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides programmably variable delay of a differential ECL input signal. It has similar architecture to the EP195 with the added feature of further tuneability in delay using the FTUNE pin. The FTUNE input takes an analog voltage from VCC to VEE to fine tune the output delay from 0 to 60 ps.

### Features

- Maximum Frequency > 1.2 GHz Typical
- PECL Mode Operating Range: VCC = 3.0 V to 3.6 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0 V to -3.6 V
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the ENbar Pin Will Force Q to Logic Low
- D[0:10] Can Accept Either ECL, LVCMOS, or LVTTTL Inputs
- VBB Output Reference Voltage
- Pb-Free Packages are Available

### Part Electrical Specifications

Product	Pricing (\$/Unit)	Compliance	Status	Input Level	Output Level	V <sub>CC</sub> Typ (V)	f <sub>Max</sub> Typ (MHz)	t <sub>d(prog)</sub> Min (ns)	t <sub>d(prog)</sub> Max (ns)	t <sub>d(step)</sub> Typ (ps)	t <sub>jitter</sub> Typ (ps)	t <sub>r</sub> & t <sub>f</sub> Max (ps)	Package Type
MC100EP196FAG		Pb-free Halide free	Active	CML ECL	ECL	3.3	1200	8.6	12	11	3	200	LQFP-32
MC100EP196FAR2G		Pb-free Halide free	Active	ECL CML	ECL	3.3	1200	8.6	12	11	3	200	LQFP-32

For more information please contact your local sales support at [www.onsemi.com](http://www.onsemi.com).

Created on: 1/28/2020