Product Overview

MC100EP31: ECL D Flip-Flop with Set and Reset

For complete documentation, see the data sheet.

The MC10/100EP31 is a D flip-flop with set and reset. The device is pin and functionally equivalent to the EL31 and LVEL31 devices. With AC performance much faster than the EL31 and LVEL31 devices, the EP31 is ideal for applications requiring the fastest AC performance available. Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when CLK is low and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK.The 100 Series contains temperature compensation.

Features

- 340ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: VCC= 3.0 V to 5.5 Vwith VEE= 0 V
- NECL Mode Operating Range: VCC= 0 Vwith VEE= –3.0 V to –5.5 V
- Open Input Default State
- Q Output will default LOW with inputs open or at VEE
- Pb-Free Packages are Available

Applications

- Clock Distribution

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Bits	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} Typ (ps)	t_{pd} Typ (ns)	t_{su} Min (ns)	t_h Min (ns)	t_{rec} Typ (ns)	t_R & t_F Max (ps)	f_{Toggle} Typ (MHz)	Package Type
MC100EP31DG		Pb-free Halide free	Active	D-Type	1	ECL CML	ECL	5 3.3	0.2	0.34	0.1	0.15	0.225	180	3000	SOIC-8
MC100EP31DTG		Pb-free Halide free	Active	D-Type	1	CML ECL	ECL	3.3 5	0.2	0.34	0.1	0.15	0.225	180	3000	TSSOP-8

For more information please contact your local sales support at www.onsemi.com.

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