Product Overview

MC100EP142: ECL 9-Bit Shift Register

For complete documentation, see the data sheet.

The MC10EP/100EP142 is a 9-bit shift register, designed with byte-parity applications in mind. The E142 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D0 - D8 accept parallel input data, while S-IN accepts serial input data. The Qn outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any Q output not used should be left unterminated.The SEL (Select) input pin is used to switch between the two modes of operation - SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK0 or CLK1; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the resisters to zero.The 100 Series contains temperature compensation.

Features

- > 3 GHz Minimum Shift Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- PECL Mode Operating Range: VCC = 3.0 V to 5.5 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = –3.0 V to –5.5 V
- Open Input Default State
- Safety Clamp on Inputs

Applications

- Byte parity

Part Electrical Specifications

Product	Compliance	Status	Type	Bits	Input Level	Output Level	V_{CC} Typ (V)	t_{Jitter} Typ (ps)	t_{pd} Typ (ns)	t_{su} Min (ns)	t_h Min (ns)	t_{rec} Typ (ns)	t_R & t_F Max (ps)	f_{Toggle} Typ (MHz)	Package Type
MC100EP142FAG	Pb-free Halide free	Active	Shift Register	9	CML ECL	ECL	3.3 5	1	0.675	0.05	0.1	0.8	250	2800	LQFP-32

For more information please contact your local sales support at www.onsemi.com.

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