Product Overview

NB6L16: Clock / Data Receiver / Driver / Translator Buffer, 2.5 V / 3.3 V Multilevel Input to Differential LVPECL/LVNECL

For complete documentation, see the data sheet.

The NB6L16 is a high precision, low power ECL differential clock or data receiver/driver/translator buffer. The device is functionally equivalent to the EL16, EP16, LVEL16 and NBSG16 devices. With output transition times of 70 ps, it is ideally suited for high frequency, low power systems. The device is targeted for Backplane buffering, GbE clock/data distribution, Fibre Channel distribution and SONET clock/data distribution applications.Input accept LVNECL (Negative ECL), LVPECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. Outputs are 800 mV ECL signals.The VBB pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01 mF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB should be left open.

Features

- Input Clock Frequency 6 GHz
- Input Data Rate Frequency 6 Gb/s
- Low 12 mA Typical Power Supply Current
- 70 ps Typical Rise/Fall Times
- 130 ps Input Propagation Delay
- On-Chip Reference for ECL Single-Ended Input - VBB Output
- PECL Mode Operating Range: VCC = 2.375 V to 3.465 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 with VEE = 2.375 V to 3.465 V
- Open Input Default State
- LVDS, LVPECL, LVNECL, LVCMOS, LVTTL and CML Input Compatible

  For more features, see the data sheet

Applications

- Backplane Data buffering
- Signal Translation Between LVDS, CML, LVTTL or LVCMOS to LVPECL

For more information please contact your local sales support at www.onsemi.com.

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