Product Overview

MC10EP32: 3.3 V / 5.0 V ECL ÷2 Divider

For complete documentation, see the data sheet.

The MC10/100EP32 is an integrated divide by 2 divider with differential CLK inputs.The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01µF capacitor and limit current sourcing or sinking to 0.5mA. When not used, VBB should be left open.The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EP32's in a system.The 100 Series contains temperature compensation.

Features

- 350ps Typical Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode Operating Range: VCC= 3.0 V to 5.5 Vwith VEE= 0 V
- NECL Mode Operating Range: VCC= 0 Vwith VEE= –3.0 V to –5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output will default LOW with inputs open or at VEE
- Pb-Free Packages are Available

Applications

- Reduce System clock skew over the alternative CMOS and TTL technologies.

Part Electrical Specifications

Product	Pricing ($/Unit)	Compliance	Status	Type	Input Level	Output Level	V_{CC} Typ (V)	f_{Max} Typ (MHz)	t_{pd} Typ (ns)	t_R & t_F Max (ps)	Package Type
MC10EP32DG		Pb-free Halide free	Active	Divider	ECL CML	ECL	5 3.3	4000	0.35	150	SOIC-8
MC10EP32DR2G		Pb-free Halide free	Active	Divider	CML ECL	ECL	5 3.3	4000	0.35	150	SOIC-8
MC10EP32DTG		Pb-free Halide free	Active	Divider	CML ECL	ECL	5 3.3	4000	0.35	150	TSSOP-8
MC10EP32DTR2G		Pb-free Halide free	Active	Divider	ECL CML	ECL	5 3.3	4000	0.35	150	TSSOP-8

For more information please contact your local sales support at www.onsemi.com.

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