# Product Overview

## MC100LVEL39: 3.3 V ECL ÷·2/4, ÷·4/6 Clock Generation Chip

For complete documentation, see the data sheet.

The MC100LVEL39 is a low skew  2/4,  4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal. In addition, by using the VBB output, a sinusoidal source can be AC coupled into the device. The common enable (ENbar) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input. Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL39s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the  2/4 and the  4/6 outputs of a single device. The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01 F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB should be left open.

## Features

- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: VCC = 3.0 V to 3.8 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = -3.0 V to -3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34

  For more features, see the data sheet

## Part Electrical Specifications

| Product | Compliance | Status | Type | Input Level | Output Level | $V_{CC}$ Typ (V) | $f_{Max}$ Typ (MHz) | $t_{pd}$ Typ (ns) | $t_R$ & $t_F$ Max (ps) | Package Type |
|---|---|---|---|---|---|---|---|---|---|---|
| MC100LVEL39DWR2G | Pb-free<br>Halide free | Active | Divider | ECL<br>LVDS | ECL | 3.3 | 1000 | 1.05 | 550 | SOIC-20W |

**For more information please contact your local sales support at www.onsemi.com.**

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