

## Product Overview

### MC100EP33: 3.3 V / 5.0 V ECL $\pm$ 4 Divider

For complete documentation, see the data sheet.

The MC10/100EP33 is an integrated divide by 4 divider. The differential clock inputs. The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01 uF capacitor and limit current sourcing or sinking to 0.5mA. When not used, VBB should be left open. The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EP33's in a system. The 100 Series contains temperature compensation.

### Features

- 320ps Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode Operating Range: VCC= 3.0 V to 5.5 V with VEE= 0 V
- NECL Mode Operating Range: VCC= 0 V with VEE= -3.0 V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output will default LOW with inputs open or at VEE
- VBB Output
- Pb-Free Packages are Available

### Applications

- Phase Lock Loops

### Part Electrical Specifications

Product	Pricing (\$/Unit)	Compliance	Status	Type	Input Level	Output Level	V <sub>CC</sub> Typ (V)	f <sub>Max</sub> Typ (MHz)	t <sub>pd</sub> Typ (ns)	t <sub>r</sub> & t <sub>f</sub> Max (ps)	Package Type
MC100EP33DG		Pb-free	Active	Divider	ECL	ECL	3.3	4000	0.38	200	SOIC-8
		Halide free			CML		5				
MC100EP33DTG		Pb-free	Active	Divider	ECL	ECL	5	4000	0.38	200	TSSOP-8
		Halide free			CML		3.3				
MC100EP33DTR2G		Pb-free	Active	Divider	CML	ECL	5	4000	0.38	200	TSSOP-8
		Halide free			ECL		3.3				
MC100EP33MNR4G		Pb-free	Active	Divider	ECL	ECL	3.3	4000	0.38	200	DFN-8
		Halide free			CML		5				

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