Low Voltage Precision Adjustable Shunt Regulator

TLV431, NCV431, SCV431

The TLV431A, B and C series are precision low voltage shunt regulators that are programmable over a wide voltage range of 1.24 V to 16 V. The TLV431A series features a guaranteed reference accuracy of ±1.0% at 25°C and ±2.0% over the entire industrial temperature range of −40°C to 85°C. The TLV431B series features higher reference accuracy of ±0.5% and ±1.0% respectively. For the TLV431C series, the accuracy is even higher. It is ±0.2% and ±1.0% respectively. These devices exhibit a sharp low current turn-on characteristic with a low dynamic impedance of 0.20 Ω over an operating current range of 100 µA to 20 mA. This combination of features makes this series an excellent replacement for zener diodes in numerous applications circuits that require a precise reference voltage. When combined with an optocoupler, the TLV431A/B/C can be used as an error amplifier for controlling the feedback loop in isolated low output voltage (3.0 V to 3.3 V) switching power supplies. These devices are available in economical TO–92–3 and micro size TSOP–5 and SOT–23–3 packages.

Features

- Programmable Output Voltage Range of 1.24 V to 16 V
- Voltage Reference Tolerance ±1.0% for A Series, ±0.5% for B Series and ±0.2% for C Series
- Sharp Low Current Turn–On Characteristic
- Low Dynamic Output Impedance of 0.20 Ω from 100 µA to 20 mA
- Wide Operating Current Range of 50 µA to 20 mA
- Micro Miniature TSOP–5, SOT–23–3 and TO–92–3 Packages
- NCV and SCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These are Pb–Free and Halide–Free Devices

Applications

- Low Output Voltage (3.0 V to 3.3 V) Switching Power Supply Error Amplifier
- Adjustable Voltage or Current Linear and Switching Power Supplies
- Voltage Monitoring
- Current Source and Sink Circuits
- Analog and Digital Circuits Requiring Precision References
- Low Voltage Zener Diode Replacements

Figure 1. Representative Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

DEVICE MARKING INFORMATION AND PIN CONNECTIONS

See general marking information in the device marking section on page 13 of this data sheet.
The device contains 13 active transistors.

**Figure 2. Representative Device Symbol and Schematic Diagram**

### MAXIMUM RATINGS

(Full operating ambient temperature range applies, unless otherwise noted)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cathode to Anode Voltage</td>
<td>$V_{KA}$</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Cathode Current Range, Continuous</td>
<td>$I_K$</td>
<td>–20 to 25</td>
<td>mA</td>
</tr>
<tr>
<td>Reference Input Current Range, Continuous</td>
<td>$I_{ref}$</td>
<td>–0.05 to 10</td>
<td>mA</td>
</tr>
<tr>
<td>Thermal Characteristics</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LP Suffix Package, TO–92–3 Package</td>
<td>$R_{IJA}$</td>
<td>178</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Ambient</td>
<td>$R_{IJC}$</td>
<td>83</td>
<td></td>
</tr>
<tr>
<td>SN Suffix Package, TSOP–5 Package</td>
<td>$R_{IJA}$</td>
<td>226</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Ambient</td>
<td>$R_{IJA}$</td>
<td>491</td>
<td></td>
</tr>
<tr>
<td>SN1 Suffix Package, SOT–23–3 Package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$T_J$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>$T_A$</td>
<td>–40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–40 to 125</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{SLP}$</td>
<td>–65 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**NOTE:** This device series contains ESD protection and exceeds the following tests:

- Human Body Model 2000 V per JEDEC JESD22–A114F, Machine Model Method 200 V per JEDEC JESD22–A115C,
- Charged Device Method 1000 V per JEDEC JESD22–C101E. This device contains latch–up protection and exceeds ±100 mA per JEDEC standard JESD78.

\[
| P_D | = \frac{T_{J(max)} - T_A}{R_{IJA}} |
\]

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cathode to Anode Voltage</td>
<td>$V_{KA}$</td>
<td>$V_{Ref}$</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>Cathode Current</td>
<td>$I_K$</td>
<td>0.1</td>
<td>20</td>
<td>mA</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>TLV431A</th>
<th>TLV431B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>Reference Voltage (Figure 3)</td>
<td>V_{ref}</td>
<td>1.228</td>
<td>1.240</td>
</tr>
<tr>
<td>( V_{KA} = V_{ref} ), ( I_K = 10 , mA ), TA = 25°C</td>
<td>1.215</td>
<td>–</td>
<td>1.265</td>
</tr>
<tr>
<td>Reference Input Voltage Deviation Over Temperature (Figure 3)</td>
<td>( \Delta V_{ref} )</td>
<td>–</td>
<td>7.2</td>
</tr>
<tr>
<td>( V_{KA} = V_{ref} ), ( I_K = 10 , mA ), TA = T_{low} to T_{high}, Notes 1, 2, 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4)</td>
<td>( \frac{\Delta V_{ref}}{\Delta V_{KA}} )</td>
<td>–</td>
<td>–0.6</td>
</tr>
<tr>
<td>( V_{KA} = V_{ref} ), ( V_{ref} = 16 , V ), ( I_C = 10 , mA )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Terminal Current (Figure 4)</td>
<td>I_{ref}</td>
<td>–</td>
<td>0.15</td>
</tr>
<tr>
<td>( I_K = 10 , mA ), R1 = 10 k\Ω, R2 = open</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Input Current Deviation Over Temperature (Figure 4)</td>
<td>( \Delta I_{ref} )</td>
<td>–</td>
<td>0.04</td>
</tr>
<tr>
<td>( I_K = 10 , mA ), R1 = 10 k\Ω, R2 = open, Notes 1, 2, 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Cathode Current for Regulation (Figure 3)</td>
<td>I_{K(min)}</td>
<td>–</td>
<td>30</td>
</tr>
<tr>
<td>Off–State Cathode Current (Figure 5)</td>
<td>I_{K(off)}</td>
<td>–</td>
<td>0.01</td>
</tr>
<tr>
<td>( V_{KA} = 6.0 , V ), ( V_{ref} = 0 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{KA} = 16 , V ), ( V_{ref} = 0 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic Impedance (Figure 3)</td>
<td>(</td>
<td>Z_{KA}</td>
<td>)</td>
</tr>
</tbody>
</table>

1. Ambient temperature range: \( T_{low} = -40°C \), \( T_{high} = 85°C \).
2. Guaranteed but not tested.
3. The deviation parameters \( \Delta V_{ref} \) and \( \Delta I_{ref} \) are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.

The average temperature coefficient of the reference input voltage, \( \alpha V_{ref} \) is defined as:

\[
\alpha V_{ref} \left( \frac{ppm}{°C} \right) = \left( \frac{\frac{(\Delta V_{ref})}{V_{ref}}}{(10^6)} \right)
\]

\( \alpha V_{ref} \) can be positive or negative depending on whether \( V_{ref} \) Min or \( V_{ref} \) Max occurs at the lower ambient temperature, refer to Figure 8.

Example: \( \Delta V_{ref} = 7.2 \, mV \) and the slope is positive,

\( V_{ref} @ 25°C = 1.241 \, V \)
\( \Delta T_A = 125°C \)

\[
\alpha V_{ref} \left( \frac{ppm}{°C} \right) = \frac{0.0072}{1.241} \times 10^6 = 46 \, ppb/°C
\]

4. The dynamic impedance \( Z_{KA} \) is defined as:

\[
|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}
\]

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

\[
|Z_{KA}’| = |Z_{KA}| \times \left( 1 + \frac{R_1}{R_2} \right)
\]

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ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>TLV431C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Voltage (Figure 3)</td>
<td>Vref</td>
<td>Min: 1.237, Typ: 1.240, Max: 1.243</td>
</tr>
<tr>
<td>(VKA = Vref, IK = 10 mA, TA = 25°C)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(TA = Tlow to Thigh, Note 5)</td>
<td></td>
<td>1.228</td>
</tr>
<tr>
<td>Reference Input Voltage Deviation Over Temperature (Figure 3)</td>
<td>△Vref</td>
<td>–</td>
</tr>
<tr>
<td>(VKA = Vref, IK = 10 mA, TA = Tlow to Thigh, Notes 5, 6, 7)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4)</td>
<td>△Vref</td>
<td>–</td>
</tr>
<tr>
<td>(VKA = Vref to 16 V, IK = 10 mA)</td>
<td>△VKA</td>
<td></td>
</tr>
<tr>
<td>Reference Terminal Current (Figure 4)</td>
<td>Iref</td>
<td>–</td>
</tr>
<tr>
<td>(IK = 10 mA, R1 = 10 kΩ, R2 = open)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Input Current Deviation Over Temperature (Figure 4)</td>
<td>△Iref</td>
<td>–</td>
</tr>
<tr>
<td>(IK = 10 mA, R1 = 10 kΩ, R2 = open, Notes 5, 6, 7)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Cathode Current for Regulation (Figure 3)</td>
<td>I_K(min)</td>
<td>–</td>
</tr>
<tr>
<td>Off–State Cathode Current (Figure 5)</td>
<td>I_K(off)</td>
<td>–</td>
</tr>
<tr>
<td>(VKA = 6.0 V, Vref = 0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(VKA = 16 V, Vref = 0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic Impedance (Figure 3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(VKA = Vref, IK = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 8)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5. Ambient temperature range: Tlow = −40°C, Thigh = 85°C.
6. Guaranteed but not tested.
7. The deviation parameters △Vref and △Iref are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.

The average temperature coefficient of the reference input voltage, αVref is defined as:

\[
αV_{ref} = \frac{(ΔV_{ref})}{V_{ref}(TA = 25°C) × 10^6 / ΔT_A}
\]

αVref can be positive or negative depending on whether Vref Min or Vref Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ∆Vref = 7.2 mV and the slope is positive,

\[
V_{ref} @ 25°C = 1.241 V
\]

\[
ΔT_A = 125°C
\]

\[
αV_{ref} = \frac{7.2}{1.241 × 10^6} = 46 \text{ ppm/°C}
\]

8. The dynamic impedance Z_KA is defined as:

\[
|Z_{KA}| = \frac{ΔV_{KA}}{ΔI_K}
\]

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

\[
|Z_{KA}'| = |Z_{KA}| × \left(1 + \frac{R1}{R2}\right)
\]
ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted. NCV prefix indicates TSOP package device. SCV prefix indicates SOT–23 package device.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>NCV431A, SCV431A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Characteristic</strong></td>
<td><strong>Symbol</strong></td>
<td><strong>Min</strong></td>
</tr>
<tr>
<td>Reference Voltage (Figure 3) (VA = Vref, IK = 10 mA, TA = 25°C)</td>
<td>Vref</td>
<td>1.228</td>
</tr>
<tr>
<td>(TA = 0°C to 125°C)</td>
<td></td>
<td>1.211</td>
</tr>
<tr>
<td>Reference Input Voltage Deviation Over Temperature (Figure 3)</td>
<td>ΔVref</td>
<td>–</td>
</tr>
<tr>
<td>(VA = Vref, IK = 10 mA, TA = 25°C, Notes 9, 10)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>(VA = Vref, IK = 10 mA, TA = 40°C to 125°C, Notes 9, 10)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4)</td>
<td>ΔVref</td>
<td>–</td>
</tr>
<tr>
<td>(VA = Vref to 16 V, IK = 10 mA)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Reference Terminal Current (Figure 4)</td>
<td>Iref</td>
<td>–</td>
</tr>
<tr>
<td>(IK = 10 mA, R1 = 10 kΩ, R2 = open)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Reference Input Current Deviation Over Temperature (Figure 4)</td>
<td>ΔIref</td>
<td>–</td>
</tr>
<tr>
<td>(IK = 10 mA, R1 = 10 kΩ, R2 = open, TA = 40°C to 125°C, Notes 9, 10)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Minimum Cathode Current for Regulation (Figure 3)</td>
<td>IK(min)</td>
<td>–</td>
</tr>
<tr>
<td>Off-State Cathode Current (Figure 5)</td>
<td>IK(off)</td>
<td>–</td>
</tr>
<tr>
<td>(VA = 6.0 V, Vref = 0)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>(VA = 16 V, Vref = 0)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>Dynamic Impedance (Figure 3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(VA = Vref, IK = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 11)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>The average temperature coefficient of the reference input voltage, αVref is</td>
<td></td>
<td></td>
</tr>
<tr>
<td>defined as:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>αVref (ppm/°C) = ( \frac{\Delta V_{\text{ref}}}{V_{\text{ref}} (T_\text{A} = 25°C)} \times 10^6 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>αVref can be positive or negative depending on whether Vref Min or Vref Max</td>
<td></td>
<td></td>
</tr>
<tr>
<td>occurs at the lower ambient temperature, refer to Figure 8. Example: ΔVref</td>
<td></td>
<td></td>
</tr>
<tr>
<td>= 7.2 mV and the slope is positive, Vref @ 25°C = 1.241 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔT_A = 125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \alpha_{V_{\text{ref}}} (\text{ppm/°C}) = \frac{0.0072}{1.241} \times 10^6 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11. The dynamic impedance ZKA is defined as:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Z\text{KA}</td>
<td>=</td>
</tr>
<tr>
<td>When the device is operating with two external resistors, R1 and R2, (refer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>to Figure 4) the total dynamic impedance of the circuit is given by:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Z\text{KA}</td>
<td>=</td>
</tr>
</tbody>
</table>
## ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise noted. NCV prefix indicates TSOP package device. SCV prefix indicates SOT−23 package device.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>NCV431B, SCV431B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Voltage (Figure 3)</td>
<td>V&lt;sub&gt;ref&lt;/sub&gt;</td>
<td>1.234</td>
</tr>
<tr>
<td>(V&lt;sub&gt;K&lt;/sub&gt; = V&lt;sub&gt;ref&lt;/sub&gt;, I&lt;sub&gt;K&lt;/sub&gt; = 10 mA, T&lt;sub&gt;A&lt;/sub&gt; = 25°C)</td>
<td></td>
<td>1.228</td>
</tr>
<tr>
<td>(T&lt;sub&gt;A&lt;/sub&gt; = −40°C to 85°C)</td>
<td></td>
<td>1.224</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T&lt;sub&gt;A&lt;/sub&gt; = −40°C to 125°C)</td>
</tr>
<tr>
<td>Reference Input Voltage Deviation Over Temperature (Figure 3)</td>
<td>ΔV&lt;sub&gt;ref&lt;/sub&gt;</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;K&lt;/sub&gt; = V&lt;sub&gt;ref&lt;/sub&gt;, I&lt;sub&gt;K&lt;/sub&gt; = 10 mA, T&lt;sub&gt;A&lt;/sub&gt; = 25°C, Notes 9, 10)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;K&lt;/sub&gt; = V&lt;sub&gt;ref&lt;/sub&gt;, I&lt;sub&gt;K&lt;/sub&gt; = 10 mA, T&lt;sub&gt;A&lt;/sub&gt; = −40°C to 85°C, Notes 9, 10)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V&lt;sub&gt;K&lt;/sub&gt; = V&lt;sub&gt;ref&lt;/sub&gt;, I&lt;sub&gt;K&lt;/sub&gt; = 10 mA, T&lt;sub&gt;A&lt;/sub&gt; = −40°C to 125°C, Notes 9, 10)</td>
</tr>
<tr>
<td>Reference Input Current Deviation Over Temperature (Figure 4)</td>
<td>ΔI&lt;sub&gt;ref&lt;/sub&gt;</td>
<td>–</td>
</tr>
<tr>
<td>(I&lt;sub&gt;K&lt;/sub&gt; = 10 mA, R&lt;sub&gt;1&lt;/sub&gt; = 10 kΩ, R&lt;sub&gt;2&lt;/sub&gt; = open)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(I&lt;sub&gt;K&lt;/sub&gt; = 10 mA, R&lt;sub&gt;1&lt;/sub&gt; = 10 kΩ, R&lt;sub&gt;2&lt;/sub&gt; = open, T&lt;sub&gt;A&lt;/sub&gt; = −40°C to 85°C, Notes 12, 13)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(I&lt;sub&gt;K&lt;/sub&gt; = 10 mA, R&lt;sub&gt;1&lt;/sub&gt; = 10 kΩ, R&lt;sub&gt;2&lt;/sub&gt; = open, T&lt;sub&gt;A&lt;/sub&gt; = −40°C to 125°C, Notes 12, 13)</td>
</tr>
<tr>
<td>Minimum Cathode Current for Regulation (Figure 3)</td>
<td>I&lt;sub&gt;(K)&lt;/sub&gt;(min)</td>
<td>–</td>
</tr>
<tr>
<td>Off−State Cathode Current (Figure 5)</td>
<td>I&lt;sub&gt;(K)&lt;/sub&gt;(off)</td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;K&lt;/sub&gt; = 6.0 V, V&lt;sub&gt;ref&lt;/sub&gt; = 0)</td>
<td></td>
<td>–</td>
</tr>
<tr>
<td>(V&lt;sub&gt;K&lt;/sub&gt; = 16 V, V&lt;sub&gt;ref&lt;/sub&gt; = 0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic Impedance (Figure 3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V&lt;sub&gt;K&lt;/sub&gt; = V&lt;sub&gt;ref&lt;/sub&gt;, I&lt;sub&gt;K&lt;/sub&gt; = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 14)</td>
<td></td>
<td>–</td>
</tr>
</tbody>
</table>

12. Guaranteed but not tested.
13. The deviation parameters ΔV<sub>ref</sub> and ΔI<sub>ref</sub> are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.

The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

\[
\alpha V_{\text{ref}} \left( \frac{\text{ppm}}{^\circ \text{C}} \right) = \frac{\left( \frac{\Delta V_{\text{ref}}}{V_{\text{ref}} (T_{\text{A}} = 25^\circ \text{C})} \right) \times 10^6}{\Delta T_{\text{A}}}
\]

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV<sub>ref</sub> = 7.2 mV and the slope is positive,

\[
V_{\text{ref}} @ 25^\circ \text{C} = 1.241 \text{ V}
\]

\[
\alpha V_{\text{ref}} \left( \frac{\text{ppm}}{^\circ \text{C}} \right) = \frac{0.0072 \times 10^6}{\frac{1.241}{125}} = 46 \text{ ppm/}^\circ \text{C}
\]

14. The dynamic impedance Z<sub>KA</sub> is defined as:

\[
|Z_{\text{KA}}| = \left| \frac{\Delta V_{\text{KA}}}{\Delta I_{\text{K}}} \right|
\]

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

\[
|Z_{\text{KA}}'| = |Z_{\text{KA}}| \times \left( 1 + \frac{R_1}{R_2} \right)
\]
Figure 3. Test Circuit for $V_{KA} = V_{ref}$

Figure 4. Test Circuit for $V_{KA} > V_{ref}$

Figure 5. Test Circuit for $I_{K(\text{off})}$

Figure 6. Cathode Current vs. Cathode Voltage

Figure 7. Cathode Current vs. Cathode Voltage

Figure 8. Reference Input Voltage versus Ambient Temperature

Figure 9. Reference Input Current versus Ambient Temperature
Figure 10. Reference Input Voltage Change versus Cathode Voltage

Figure 11. Off−State Cathode Current versus Cathode Voltage

Figure 12. Off−State Cathode Current versus Ambient Temperature

Figure 13. Dynamic Impedance versus Frequency

Figure 14. Dynamic Impedance versus Ambient Temperature

Figure 15. Open−Loop Voltage Gain versus Frequency
Stability

Figures 18 and 19 show the stability boundaries and circuit configurations for the worst case conditions with the load capacitance mounted as close as possible to the device. The required load capacitance for stable operation can vary depending on the operating temperature and capacitor equivalent series resistance (ESR). Ceramic or tantalum surface mount capacitors are recommended for both temperature and ESR. The application circuit stability should be verified over the anticipated operating current and temperature ranges.

### Stability Boundary Conditions

<table>
<thead>
<tr>
<th>Unstable Regions</th>
<th>$V_{KA}$ (V)</th>
<th>$R_1$ (kΩ)</th>
<th>$R_2$ (kΩ)</th>
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<tr>
<td>A, C</td>
<td>$V_{ref}$</td>
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<tr>
<td>B, D</td>
<td>5.0</td>
<td>30.4</td>
<td>10</td>
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---

www.onsemi.com
TYPICAL APPLICATIONS

Figure 20. Shunt Regulator

\[ V_{out} = \left(1 + \frac{R_1}{R_2}\right)V_{ref} \]

\[ V_{out(min)} = V_{ref} + 5.0\, \text{V} \]

Figure 21. High Current Shunt Regulator

\[ V_{out} = \left(1 + \frac{1}{R_2}\right)V_{ref} \]

Figure 22. Output Control for a Three Terminal Fixed Regulator

\[ V_{out} = \left(1 + \frac{R_1}{R_2}\right)V_{ref} \]

\[ V_{in(min)} = V_{out} + V_{be} \]

\[ V_{out(min)} = V_{ref} \]

Figure 23. Series Pass Regulator

\[ V_{in} \rightarrow \text{MC7805} \rightarrow V_{out} \]

\[ V_{in} \rightarrow R_1 \rightarrow V_{out} \]

\[ V_{in} \rightarrow R_2 \rightarrow V_{out} \]
Figure 24. Constant Current Source

\[ I_{\text{out}} = \frac{V_{\text{ref}}}{R_{\text{CL}}} \]

Figure 25. Constant Current Sink

\[ I_{\text{sink}} = \frac{V_{\text{ref}}}{R_{S}} \]

Figure 26. TRIAC Crowbar

\[ V_{\text{out(trip)}} = \left( 1 + \frac{R_{1}}{R_{2}} \right) V_{\text{ref}} \]

Figure 27. SCR Crowbar

\[ V_{\text{out(trip)}} = \left( 1 + \frac{R_{1}}{R_{2}} \right) V_{\text{ref}} \]
Figure 28. Voltage Monitor

L.E.D. indicator is ‘ON’ when $V_{in}$ is between the upper and lower limits,

Lower limit = \( \frac{1 + \frac{R_1}{R_2}}{V_{ref}} \)

Upper limit = \( \frac{1 + \frac{R_3}{R_4}}{V_{ref}} \)

Figure 29. Linear Ohmmeter

Figure 30. Simple 400 mW Phono Amplifier
Figure 31. Isolated Output Line Powered Switching Power Supply

The above circuit shows the TLV431A/B/C as a compensated amplifier controlling the feedback loop of an isolated output line powered switching regulator. The output voltage is programmed to 3.3 V by the resists values selected for R1 and R2. The minimum output voltage that can be programmed with this circuit is 2.64 V, and is limited by the sum of the reference voltage (1.24 V) and the forward drop of the optocoupler light emitting diode (1.4 V). Capacitor C1 provides loop compensation.

PIN CONNECTIONS AND DEVICE MARKING

(Note: Microdot may be in either location)
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Code</th>
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*SCV, NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.
FORMED LEAD

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

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STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER: 98AON52857E
DESCRIPTION: TO-92 (TO-226) 1 WATT
TO-92 (TO-226) 1 WATT
CASE 29−10
ISSUE D
DATE 05 MAR 2021

STYLE 1:
PIN 1. Emitter
2. Base
3. Collector

STYLE 2:
PIN 1. Base
2. Emitter
3. Collector

STYLE 3:
PIN 1. Anode
2. Anode
3. Cathode

STYLE 4:
PIN 1. Cathode
2. Anode
3. Collector

STYLE 5:
PIN 1. Drain
2. Cathode
3. Gate

STYLE 6:
PIN 1. Gate
2. Source & Substrate
3. Drain

STYLE 7:
PIN 1. Source
2. Drain
3. Gate

STYLE 8:
PIN 1. Drain
2. Source
3. Gate

STYLE 9:
PIN 1. Base 1
2. Emitter
3. Gate

STYLE 10:
PIN 1. Cathode
2. Emitter
3. Gate

STYLE 11:
PIN 1. Anode
2. Cathode & Anode
3. Cathode

STYLE 12:
PIN 1. Main Terminal 1
2. Gate
3. Main Terminal 2

STYLE 13:
PIN 1. Anode
2. Gate
3. Not Connected

STYLE 14:
PIN 1. Collector
2. Anode
3. Cathode

STYLE 15:
PIN 1. Collector
2. Gate
3. Anode

STYLE 16:
PIN 1. Collector
2. Gate
3. Cathode

STYLE 17:
PIN 1. Collector
2. Base
3. Emitter

STYLE 18:
PIN 1. Collector
2. Cathode
3. Not Connected

STYLE 19:
PIN 1. Gate
2. Anode
3. Cathode

STYLE 20:
PIN 1. Gate
2. Cathode
3. Anode

STYLE 21:
PIN 1. Collector
2. Emitter
3. Base

STYLE 22:
PIN 1. Source
2. Gate
3. Drain

STYLE 23:
PIN 1. Gate
2. Source
3. Drain

STYLE 24:
PIN 1. Collector
2. Source
3. Cathode

STYLE 25:
PIN 1. Collector
2. Cathode
3. MT 2

STYLE 26:
PIN 1. VCC
2. Ground
3. Output

STYLE 27:
PIN 1. MT
2. Substrate
3. MT

STYLE 28:
PIN 1. Cathode
2. Anode
3. Gate

STYLE 29:
PIN 1. Not Connected
2. Anode
3. Cathode

STYLE 30:
PIN 1. Drain
2. Cathode
3. Source

STYLE 31:
PIN 1. Drain
2. Collector
3. Source

STYLE 32:
PIN 1. Collector
2. Emitter
3. Output

STYLE 33:
PIN 1. Return
2. Input
3. Logic

STYLE 34:
PIN 1. Input
2. Ground
3. Collector

STYLE 35:
PIN 1. Collector
2. Output
3. EMITTER

GENERIC MARKING DIAGRAM*

XXXXX XXXXX ALYW*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
* = Pb-Free Indicator, "G" or Microdot " *

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or Microdot " *", may or may not be present. Some products may not follow the Generic Marking.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOT–23 (TO–236)
CASE 318–08
ISSUE AS

DATE 30 JAN 2018

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERAL MARKING DIAGRAM*

XXXM*

**This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot "*', may or may not be present.

DIMENSIONS: MILLIMETERS

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**PITCH**

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DIMENSIONS: MILLIMETERS

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**PITCH**

3X 0.90

RECOMMENDED SOLDERING FOOTPRINT

SIDE VIEW

TOP VIEW

VIEW C

END VIEW

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
P1. BASE
2. Emitter
3. Collector

STYLE 7:
P1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
P1. ANODE
2. CATHODE
3. BASE

STYLE 9:
P1. ANODE
2. CATHODE
3. BASE

STYLE 10:
P1. GATE
2. SOURCE
3. DRAIN

STYLE 11:
P1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 12:
P1. SOURCE
2. CATHODE
3. ANODE

STYLE 13:
P1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 14:
P1. CATHODE
2. ANODE
3. GATE

STYLE 15:
P1. GATE
2. CATHODE
3. ANODE

STYLE 16:
P1. CATHODE
2. SOURCE
3. DRAM

STYLE 17:
P1. CATHODE
2. BASE
3. GATE

STYLE 18:
P1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
P1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 20:
P1. CATHODE
2. ANODE
3. GATE

STYLE 21:
P1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
P1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
P1. ANODE
2. BASE
3. GATE

STYLE 24:
P1. ANODE
2. SOURCE
3. CATHODE

STYLE 25:
P1. ANODE
2. CATHODE
3. GATE

STYLE 26:
P1. ANODE
2. SOURCE
3. GATE

STYLE 27:
P1. CATHODE
2. BASE
3. GATE

STYLE 28:
P1. CATHODE
2. SOURCE
3. DRAM

**STYLE 1 THROUGH 5: CANCELLED**

**STYLE 6:**
- P1. BASE
- P2. Emitter
- P3. Collector

**STYLE 7:**
- P1. EMITTER
- P2. BASE
- P3. COLLECTOR

**STYLE 8:**
- P1. ANODE
- P2. CATHODE
- P3. BASE

**STYLE 9:**
- P1. ANODE
- P2. CATHODE
- P3. BASE

**STYLE 10:**
- P1. GATE
- P2. SOURCE
- P3. DRAIN

**STYLE 11:**
- P1. NO CONNECTION
- P2. CATHODE
- P3. ANODE

**STYLE 12:**
- P1. SOURCE
- P2. CATHODE
- P3. ANODE

**STYLE 13:**
- P1. CATHODE
- P2. ANODE
- P3. NO CONNECTION

**STYLE 14:**
- P1. CATHODE
- P2. ANODE
- P3. GATE

**STYLE 15:**
- P1. GATE
- P2. CATHODE
- P3. ANODE

**STYLE 16:**
- P1. CATHODE
- P2. SOURCE
- P3. DRAIN

**STYLE 17:**
- P1. CATHODE
- P2. BASE
- P3. GATE

**STYLE 18:**
- P1. NO CONNECTION
- P2. CATHODE
- P3. ANODE

**STYLE 19:**
- P1. NO CONNECTION
- P2. CATHODE
- P3. ANODE

**STYLE 20:**
- P1. CATHODE
- P2. ANODE
- P3. GATE

**STYLE 21:**
- P1. GATE
- P2. SOURCE
- P3. DRAIN

**STYLE 22:**
- P1. RETURN
- P2. OUTPUT
- P3. INPUT

**STYLE 23:**
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- P2. BASE
- P3. GATE

**STYLE 24:**
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- P2. SOURCE
- P3. CATHODE

**STYLE 25:**
- P1. ANODE
- P2. CATHODE
- P3. GATE

**STYLE 26:**
- P1. ANODE
- P2. SOURCE
- P3. CATHODE

**STYLE 27:**
- P1. CATHODE
- P2. BASE
- P3. GATE

**STYLE 28:**
- P1. CATHODE
- P2. SOURCE
- P3. DRAIN
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

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</tbody>
</table>

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “*”, may or may not be present.