Programmable Precision References

TL431A, B Series, NCV431A, B Series, SCV431A

The TL431A, B integrated circuits are three-termed shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from $V_{\text{ref}}$ to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 $\Omega$. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

Features
- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: $\pm 0.4\%$, Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22 $\Omega$ Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ORDERING INFORMATION
See detailed ordering and shipping information on page 13 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 14 of this data sheet.
Figure 1. Symbol

Figure 2. Representative Block Diagram

This device contains 12 active transistors.

Figure 3. Representative Schematic Diagram

Component values are nominal

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cathode to Anode Voltage</td>
<td>$V_{KA}$</td>
<td>37</td>
<td>V</td>
</tr>
<tr>
<td>Cathode Current Range, Continuous</td>
<td>$I_K$</td>
<td>−100 to +150</td>
<td>mA</td>
</tr>
<tr>
<td>Reference Input Current Range, Continuous</td>
<td>$I_{ref}$</td>
<td>−0.05 to +10</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>$T_J$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>$T_A$</td>
<td>−40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>TL431I, TL431AI, TL431BI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TL431C, TL431AC, TL431BC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCV431AI, NCV431B, TL431BV, SCV431AI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Total Power Dissipation @ $T_A = 25°C</td>
<td>$P_D$</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>Derate above 25°C Ambient Temperature</td>
<td></td>
<td>0.70</td>
<td></td>
</tr>
<tr>
<td>D, LP Suffix Plastic Package</td>
<td></td>
<td>1.10</td>
<td></td>
</tr>
<tr>
<td>P Suffix Plastic Package</td>
<td></td>
<td>0.52</td>
<td></td>
</tr>
<tr>
<td>DM Suffix Plastic Package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Power Dissipation @ $T_C = 25°C</td>
<td>$P_D$</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>Derate above 25°C Case Temperature</td>
<td></td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>D, LP Suffix Plastic Package</td>
<td></td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td>P Suffix Plastic Package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Rating (Note 1)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human Body Model per JEDEC JESD22–A114F</td>
<td>HBM</td>
<td>&gt;2000</td>
<td>V</td>
</tr>
<tr>
<td>Machine Model per JEDEC JESD22–A115C</td>
<td>MM</td>
<td>&gt;200</td>
<td></td>
</tr>
<tr>
<td>Charged Device Model per JEDEC JESD22–C101E</td>
<td>CDM</td>
<td>&gt;500</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch-up protection and exceeds ±100 mA per JEDEC standard JESD78.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cathode to Anode Voltage</td>
<td>$V_{KA}$</td>
<td>$V_{ref}$</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Cathode Current</td>
<td>$I_K$</td>
<td>1.0</td>
<td>100</td>
<td>mA</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
**THERMAL CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>D, LP Suffix Package</th>
<th>P Suffix Package</th>
<th>DM Suffix Package</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, Junction–to–Ambient</td>
<td>R_{UA}</td>
<td>178</td>
<td>114</td>
<td>240</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Case</td>
<td>R_{UC}</td>
<td>83</td>
<td>41</td>
<td>–</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>TL431I</th>
<th>TL431C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Input Voltage (Figure 1)</td>
<td>V_{ref}</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{KA} = V_{ref}, I_{k} = 10 mA</td>
<td>2.44</td>
<td>2.495</td>
<td>2.55</td>
<td>V</td>
</tr>
<tr>
<td>T_A = T_{low} to T_{high} (Note 2)</td>
<td>2.41</td>
<td>2.58</td>
<td>2.423</td>
<td>V</td>
</tr>
<tr>
<td>Reference Input Voltage Deviation Over</td>
<td>ΔV_{ref}</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Temperature Range (Figure 1, Notes 3, 4)</td>
<td></td>
<td>−7.0</td>
<td>30</td>
<td>mV</td>
</tr>
<tr>
<td>V_{KA} = V_{ref}, I_{k} = 10 mA</td>
<td>−1.4</td>
<td>−2.7</td>
<td>−1.4</td>
<td>mV</td>
</tr>
<tr>
<td>Ratio of Change in Reference Input Voltage to</td>
<td>ΔV_{ref}</td>
<td></td>
<td></td>
<td>mV/V</td>
</tr>
<tr>
<td>Change</td>
<td></td>
<td>−1.0</td>
<td>−2.0</td>
<td>mV/V</td>
</tr>
<tr>
<td>in Cathode to Anode Voltage</td>
<td></td>
<td>−1.4</td>
<td>−2.7</td>
<td>mV/V</td>
</tr>
<tr>
<td>Reference Input Current (Figure 2)</td>
<td>I_{ref}</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>I_{k} = 10 mA, R_1 = 10 k, R_2 = ∞</td>
<td>−1.8</td>
<td>4.0</td>
<td>−1.8</td>
<td>μA</td>
</tr>
<tr>
<td>T_A = 25°C</td>
<td>−6.5</td>
<td>−5.2</td>
<td>−6.5</td>
<td>μA</td>
</tr>
<tr>
<td>Reference Input Deviation Over</td>
<td>ΔI_{ref}</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Temperature Range (Figure 2, Note 3)</td>
<td></td>
<td>−0.8</td>
<td>2.5</td>
<td>μA</td>
</tr>
<tr>
<td>V_{KA} = V_{ref} (Figure 1)</td>
<td>0.5</td>
<td>1.0</td>
<td>0.5</td>
<td>μA</td>
</tr>
<tr>
<td>Minimum Cathode Current For Regulation</td>
<td>I_{min}</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>V_{KA} = V_{ref} (Figure 1)</td>
<td>−0.5</td>
<td>1.0</td>
<td>−0.5</td>
<td>mA</td>
</tr>
<tr>
<td>Off–State Cathode Current (Figure 3)</td>
<td>I_{off}</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>V_{KA} = 36 V, V_{ref} = 0 V</td>
<td>20</td>
<td>1000</td>
<td>20</td>
<td>nA</td>
</tr>
<tr>
<td>Dynamic Impedance (Figure 1, Note 5)</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>V_{KA} = V_{ref}, ΔI_{k} = 1.0 mA to 100 mA, f ≤ 1.0 kHz</td>
<td>0.22</td>
<td>0.5</td>
<td>0.22</td>
<td>Ω</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.


3. Guaranteed by design.

4. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.

5. The dynamic impedance Z_{KA} is defined as: |Z_{KA}| = ΔV_{KA}/ΔI_{k}. When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as: |Z_{KA}| = |Z_{KA}|(1 + R1/R2).
ELECTRICAL CHARACTERISTICS \( (T_A = 25^\circ \text{C}, \text{unless otherwise noted}) \)

| Characteristic                                                                 | Symbol      | \begin{tabular}{c|cccc|cccc|cccc} \hline  
|                                                                              | TL431AI / & | TL431AC / & | TL431BC / & | TL431BI / & | Unit      
|                                                                              | NCV431AI / & | NCV431AI / & | NCV431BI / & | NCV431BI / & |           
|                                                                              | SCV431AI   | SCV431AC   | SCV431BI   | SCV431BI   |           
|                                                                              |            |            |            |            |           
| Reference Input Voltage (Figure 1)                                          | \( V_{\text{ref}} \) | 2.47       | 2.495      | 2.52       | 2.47       | 2.495      | 2.52       | 2.485      | 2.495      | 2.505      | V          
| \( V_{\text{KA}} = V_{\text{ref}}, \, I_K = 10 \, \text{mA} \)             |            | 2.44       | \(-\)       | 2.55       | 2.453      | \(-\)       | 2.537      | 2.475      | 2.495      | 2.515      
| \( T_A = 25^\circ \text{C} \)                                               |            |            |            |            |            |            |            |            |            |            
| \( T_A = T_{\text{low}} \) to \( T_{\text{high}} \) (Note 6)               |            |            |            |            |            |            |            |            |            |            
| Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 7, 8) | \( \Delta V_{\text{ref}} \) | \(-\)       | 7.0        | 30         | \(-\)       | 3.0        | 17         | \(-\)       | 3.0        | 17         | mV         
| \( V_{\text{KA}} = V_{\text{ref}}, \, I_K = 10 \, \text{mA} \)             |            |            |            |            |            |            |            |            |            |            
| Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage | \( \frac{\Delta V_{\text{ref}}}{\Delta V_{\text{KA}}} \) | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | mV/V       
| \( I_K = 10 \, \text{mA} \) (Figure 2), \( \Delta V_{\text{KA}} = 10 \, \text{V to} \, V_{\text{ref}} \) |            | \(-\)       | \(-1.4\)   | \(-2.7\)   | \(-\)       | \(-1.4\)   | \(-2.7\)   | \(-\)       | \(-1.4\)   | \(-2.7\)   
| \( \Delta V_{\text{KA}} = 36 \, \text{V to} \, 10 \, \text{V} \)           |            | \(-\)       | \(-1.0\)   | \(-2.0\)   | \(-\)       | \(-1.0\)   | \(-2.0\)   | \(-\)       | \(-1.0\)   | \(-2.0\)   
| Reference Input Current (Figure 2)                                          | \( I_{\text{ref}} \) | \(-\)       | 0.8        | 2.5        | \(-\)       | 0.4        | 1.2        | \(-\)       | 0.8        | 2.5        | \( \mu \text{A} \) 
| \( I_K = 10 \, \text{mA}, \, R_1 = 10 \, \text{k}\Omega, \, R_2 = \infty \) |            | \(-\)       | 1.8        | 4.0        | \(-\)       | 1.8        | 4.0        | \(-\)       | 1.1        | 2.0        
| \( T_A = 25^\circ \text{C} \)                                               |            | \(-\)       | 6.5        | \(-\)       | \(-\)       | 5.2        | \(-\)       | \(-\)       | 4.0        
| Reference Input Current Deviation Over Temperature Range (Figure 2, Note 7)  | \( \Delta I_{\text{ref}} \) | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \( \mu \text{A} \) 
| \( I_K = 10 \, \text{mA}, \, R_1 = 10 \, \text{k}\Omega, \, R_2 = \infty \) |            | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       | \(-\)       
| \( V_{\text{KA}} = V_{\text{ref}} \) (Figure 1)                            | \( I_{\text{min}} \) | \(-\)       | 0.5        | 1.0        | \(-\)       | 0.5        | 1.0        | \(-\)       | 0.5        | 1.0        | mA         
| Minimum Cathode Current For Regulation \( V_{\text{KA}} = V_{\text{ref}} \) (Figure 1) | \( I_{\text{off}} \) | \(-\)       | 0.2        | 10000      | \(-\)       | 0.2        | 10000      | \(-\)       | 0.2        | 500        | nA         
| Off-State Cathode Current (Figure 3)                                        | \( |Z_{\text{KA}}| \) | 0.22       | 0.5        | \(-\)       | 0.22       | 0.5        | \(-\)       | 0.14       | 0.3        | \( \Omega \) 
| \( V_{\text{KA}} = V_{\text{ref}}, \, \Delta K = 1.0 \, \text{mA to} \, 100 \, \text{mA} \) |  | \( f \leq 1.0 \, \text{kHz} \) | | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.


7. \( T_{\text{high}} = +85^\circ \text{C} \) for TL431AI P TL431AILP, TL431IP, TL431ILP, TL431BIP, TL431BILP, TL431BV, TL431BID, TL431BIDM, TL431BDM, TL431BDM, TL431BIDM, TL431BDM, TL431BDM, TL431BDM

8. \( T_{\text{low}} = +85^\circ \text{C} \) for TL431AI P TL431AILP, TL431IP, TL431ILP, TL431BIP, TL431BILP, TL431BV, TL431BID, TL431BIDM, TL431BDM, TL431BDM, TL431BDM, TL431BDM, TL431BDM, TL431BDM

9. \( \alpha V_{\text{ref}} \) can be positive or negative depending on whether \( V_{\text{ref}} \) Min or \( V_{\text{ref}} \) Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example: \( \Delta V_{\text{ref}} = 8.0 \, \text{mV} \) and slope is positive,
\( V_{\text{ref}} \) @ 25°C = 2.495 V, \( \Delta T_{A} = 70^\circ \text{C} \)
\( \alpha V_{\text{ref}} = 0.008 \times 10^{6} \left( \frac{\Delta V_{\text{ref}}}{V_{\text{ref}} @ 25^\circ \text{C}} \right) = 54.8 \, \text{ppm/C} \)

10. \( \Delta V_{\text{ref}} = 8.0 \, \text{mV} \) and slope is positive,
\( V_{\text{ref}} \) @ 25°C = 2.495 V, \( \Delta T_{A} = 70^\circ \text{C} \)
\( \alpha V_{\text{ref}} = 0.008 \times 10^{6} \left( \frac{\Delta V_{\text{ref}}}{V_{\text{ref}} @ 25^\circ \text{C}} \right) = 54.8 \, \text{ppm/C} \)

9. The dynamic impedance \( Z_{\text{KA}} \) is defined as \( |Z_{\text{KA}}| = \frac{\Delta V_{\text{KA}}}{\Delta I_{K}} \). When the device is programmed with two external resistors, \( R_1 \) and \( R_2 \), (refer to Figure 2) the total dynamic impedance of the circuit is defined as: \( |Z_{\text{KA}}| = |Z_{\text{KA}}| \left( 1 + \frac{R_1}{R_2} \right) \)
Figure 1. Test Circuit for $V_{KA} = V_{ref}$

Figure 2. Test Circuit for $V_{KA} > V_{ref}$

Figure 3. Test Circuit for $I_{off}$

Figure 4. Cathode Current versus Cathode Voltage

Figure 5. Cathode Current versus Cathode Voltage

Figure 6. Reference Input Voltage versus Ambient Temperature

Figure 7. Reference Input Current versus Ambient Temperature
Figure 8. Change in Reference Input Voltage versus Cathode Voltage

Figure 9. Off-State Cathode Current versus Ambient Temperature

Figure 10. Dynamic Impedance versus Frequency

Figure 11. Dynamic Impedance versus Ambient Temperature

Figure 12. Open-Loop Voltage Gain versus Frequency

Figure 13. Spectral Noise Density
Figure 20. Output Control for a Three-Terminal Fixed Regulator

\[ V_{out} = \left( 1 + \frac{R_1}{R_2} \right) V_{ref} \]
\[ V_{out(min)} = V_{ref} + 5.0 \text{ V} \]

Figure 21. Series Pass Regulator

\[ V_{out} = \left( 1 + \frac{R_1}{R_2} \right) V_{ref} \]
\[ V_{in(min)} = V_{out} + V_{be} \]
\[ V_{out(min)} = V_{ref} \]

Figure 22. Constant Current Source

\[ I_{out} = \frac{V_{ref}}{R_{CL}} \]

Figure 23. Constant Current Sink

\[ I_{Sink} = \frac{V_{ref}}{R_S} \]

Figure 24. TRIAC Crowbar

\[ V_{out(trip)} = \left( 1 + \frac{R_1}{R_2} \right) V_{ref} \]

Figure 25. SRC Crowbar

\[ V_{out(trip)} = \left( 1 + \frac{R_1}{R_2} \right) V_{ref} \]
Figure 26. Voltage Monitor

L.E.D. indicator is ‘on’ when V+ is between the upper and lower limits.

Lower Limit = \( 1 + \frac{R_1}{R_2} \) \( V_{\text{ref}} \)

Upper Limit = \( 1 + \frac{R_3}{R_4} \) \( V_{\text{ref}} \)

Figure 27. Single-Supply Comparator with Temperature-Compensated Threshold

\[
\begin{array}{c|c}
V_{\text{in}} & V_{\text{out}} \\
\hline
< V_{\text{ref}} & V_+ \\
> V_{\text{ref}} & = 2.0 \text{ V} \\
\end{array}
\]

Figure 28. Linear Ohmmeter

\( V_{\text{out}} = \frac{R_x}{R_{\text{Range}}} \cdot V_{\text{Range}} \)

Figure 29. Simple 400 mW Phono Amplifier
Figure 30. High Efficiency Step-Down Switching Converter

<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line Regulation</td>
<td>$V_{in} = 10 \text{ V to } 20 \text{ V}, I_o = 1.0 \text{ A}$</td>
<td>53 mV (1.1%)</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$V_{in} = 15 \text{ V}, I_o = 0 \text{ A to } 1.0 \text{ A}$</td>
<td>25 mV (0.5%)</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{in} = 10 \text{ V}, I_o = 1.0 \text{ A}$</td>
<td>50 mVpp P.A.R.D.</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>$V_{in} = 20 \text{ V}, I_o = 1.0 \text{ A}$</td>
<td>100 mVpp P.A.R.D.</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$V_{in} = 15 \text{ V}, I_o = 1.0 \text{ A}$</td>
<td>82%</td>
</tr>
</tbody>
</table>
The TL431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non-standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the TL431 is shown in Figure 31. When tested for stability boundaries, the load resistance is 150Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, G_m, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of G_m flows through compensation capacitance, C_P2. The voltage across C_P2 drives the output dependent current source, G_o, which is connected across the device cathode and anode.

Model component values are:
V_ref = 1.78 V
G_m = 0.3 + 2.7 exp (-I_C/26 mA)
where I_C is the device cathode current and G_m is in mhos
G_o = 1.25 (V_{cp2}) \mu mhos.

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

\[
P_1 = \frac{1}{2\pi R_{GM} C_{P1}} = \frac{1}{2\pi \times 1.0 M \times 20 \text{ pF}} = 7.96 \text{ kHz}
\]

\[
P_2 = \frac{1}{2\pi R_{P2} C_{P2}} = \frac{1}{2\pi \times 10 M \times 0.265 \text{ pF}} = 60 \text{ kHz}
\]

\[
Z_1 = \frac{1}{2\pi R_{Z1} C_{P1}} = \frac{1}{2\pi \times 15.9 k \times 20 \text{ pF}} = 500 \text{ kHz}
\]

In addition, there is an external circuit pole defined by the load:

\[
P_L = \frac{1}{2\pi R_L C_L}
\]

Also, the transfer dc voltage gain of the TL431 is:

\[
G = G_M R_{GM} G_o R_L
\]

Example 1:
I_C = 10 mA, R_L = 230 Ω, C_L = 0. Define the transfer gain.

The DC gain is:

\[
G = G_M R_{GM} G_o R_L = (2.138)(1.0 M)(1.25 \mu)(230) = 615 = 56 \text{ dB}
\]

Loop gain = \[
\frac{8.25 k}{8.25 k + 15 k} = 218 = 47 \text{ dB}
\]

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

\[
A_v = 615 \left( 1 + \frac{jf}{500 \text{ kHz}} \right) \left( 1 + \frac{jf}{8.0 \text{ kHz}} \right) \left( 1 + \frac{jf}{60 \text{ kHz}} \right)
\]

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open–Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.
Example 2.

$I_C = 7.5 \text{ mA}$, $R_L = 2.2 \text{ k}\Omega$, $C_L = 0.01 \text{ \mu F}$. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} G_{CL} = (2.323)(1.0 M)(1.25 \mu)(2200) = 6389 = 76 \text{ dB}$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$Av = 615 \frac{1 + \frac{jf}{500 \text{ kHz}}}{(1 + \frac{jf}{8.0 \text{ kHz}})(1 + \frac{jf}{60 \text{ kHz}})(1 + \frac{jf}{7.2 \text{ kHz}})}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about ~46 degrees. Therefore, instability of this circuit is likely.

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.
### ORDERING INFORMATION

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<th>Device</th>
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<th>Operating Temperature Range</th>
<th>Package Code</th>
<th>Shipping Information</th>
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Change Requirements; AEC–Q100 Qualified and PPAP Capable.
## ORDERING INFORMATION

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<th>Package Code</th>
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

## MARKING DIAGRAMS

- **SOIC−8**
  - D Suffix
  - Case 751
  - Marking Code: TL431xxx ALYW
  - (Exception for the TL431CD and TL431ID only)

- **Micro8**
  - Case 846A
  - Marking Code: xxxx AYW
  - xxx = See Specific Marking Code
  - A = Assembly Location
  - WL, L = Wafer Lot
  - YY, Y = Year
  - WW, W = Work Week
  - *or G = Pb−Free Package
  - (Note: Microdot may be in either location)

- **PDIP−8**
  - Case 626
  - Marking Code: TL431xxx ALYW
  - (Note: Microdot may be in either location)

- **TO−92 (TO−226)**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−92**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−226**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−92**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−226**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−92**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−226**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−92**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−226**
  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−92**
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  - Case 29
  - Marking Code: TL431 xxx ALYW

- **TO−226**
  - Case 29
  - Marking Code: TL431 xxx ALYW
### TO-92 (TO-226) 1 WATT

**CASE 29-10**  
**ISSUE D**  
**DATE 05 MAR 2021**

**STRAIGHT LEAD**

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20.
DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

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</tr>
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<td>E</td>
</tr>
<tr>
<td>E2</td>
</tr>
<tr>
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**STYLES AND MARKING ON PAGE 3**

**DOCUMENT NUMBER:** 98AON52857E  
**DESCRIPTION:** TO-92 (TO-226) 1 WATT  
**PAGE 1 OF 3**

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FORMED LEAD

NOTES:
2. CONTROLLING DIMENSIONS: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20.
   DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

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STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER: 98AON52857E
DESCRIPTION: TO–92 (TO–226) 1 WATT

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www.onsemi.com
**GENERIC MARKING DIAGRAM**

```
XXXXX
XXXXX
ALYW*
```

- **XXXXX** = Specific Device Code
- **A** = Assembly Location
- **L** = Wafer Lot
- **Y** = Year
- **W** = Work Week
- **=** = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “•”, may or may not be present. Some products may not follow the Generic Marking.*
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

PDIP-8
CASE 626–05
ISSUE P

DATE 22 APR 2015

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
AGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE
NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE
LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE
LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
CORNERS).

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**GENERIC**

MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot "*", may or may not be present.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

**SOLDERING FOOTPRINT**

**GENERIC MARKING DIAGRAM**

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

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## STYLE 1:
- **PIN 1. Emitter**
- **PIN 2. Collector**
- **PIN 3. Collector**
- **PIN 4. Emitter**
- **PIN 5. Emitter**
- **PIN 6. Base**
- **PIN 7. Base**
- **PIN 8. Emitter**

## STYLE 2:
- **PIN 1. Collector, Die, #1**
- **PIN 2. Collector, #2**
- **PIN 3. Collector, #2**
- **PIN 4. Emitter, #2**
- **PIN 5. Emitter, #2**
- **PIN 6. Emitter, #2**
- **PIN 7. Base, #1**
- **PIN 8.Emitter, #1**

## STYLE 3:
- **PIN 1. Drain, Die #1**
- **PIN 2. Drain, #2**
- **PIN 3. Drain, #2**
- **PIN 4. Source, #2**
- **PIN 5. Source, #2**
- **PIN 6. Source, #2**
- **PIN 7. Gate, #1**
- **PIN 8. Source, #1**

## STYLE 4:
- **PIN 1. Anode**
- **PIN 2. Base, Die #1**
- **PIN 3. Base, Die #1**
- **PIN 4. Collector, #2**
- **PIN 5. Collector, #2**
- **PIN 6. Emitter, #2**
- **PIN 7. Anode**
- **PIN 8. Common Cathode**

## STYLE 5:
- **PIN 1. Drain**
- **PIN 2. Drain**
- **PIN 3. Drain**
- **PIN 4. Source**
- **PIN 5. Source**
- **PIN 6. Gate**
- **PIN 7. Source**
- **PIN 8. Source**

## STYLE 6:
- **PIN 1. Source**
- **PIN 2. Drain**
- **PIN 3. Drain**
- **PIN 4. Source**
- **PIN 5. Source**
- **PIN 6. Gate**
- **PIN 7. Gate**
- **PIN 8. Source**

## STYLE 7:
- **PIN 1. External Bypass**
- **PIN 2. Third Stage Source**
- **PIN 3. Ground**
- **PIN 4. Drain**
- **PIN 5. Drain**
- **PIN 6. Gate**
- **PIN 7. Second Stage Vd**
- **PIN 8. First Stage Vd**

## STYLE 8:
- **PIN 1. Collector, Die #1**
- **PIN 2. Base, #1**
- **PIN 3. Base, #2**
- **PIN 4. Collector, #2**
- **PIN 5. Collector, #2**
- **PIN 6. Emitter, #2**
- **PIN 7. Anode**
- **PIN 8. Common Cathode**

## STYLE 9:
- **PIN 1. Emitter, Common**
- **PIN 2. Collector, Die #1**
- **PIN 3. Collector, Die #2**
- **PIN 4. Emitter, Common**
- **PIN 5. Emitter, Common**
- **PIN 6. Base, Die #2**
- **PIN 7. Base, Die #1**
- **PIN 8. Emitter, Common**

## STYLE 10:
- **PIN 1. Source**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Ground**
- **PIN 5. Ground**
- **PIN 6. Bias 2**
- **PIN 7. Drain**
- **PIN 8. Drain**

## STYLE 11:
- **PIN 1. Source**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Input**
- **PIN 8. Drain**

## STYLE 12:
- **PIN 1. Source**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Input**
- **PIN 8. Drain**

## STYLE 13:
- **PIN 1. N.C.**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. N. Drain**
- **PIN 8. N. Drain**

## STYLE 14:
- **PIN 1. N. Source**
- **PIN 2. Source**
- **PIN 3. P. Source**
- **PIN 4. P. Gate**
- **PIN 5. P. Drain**
- **PIN 6. P. Drain**
- **PIN 7. N. Drain**
- **PIN 8. N. Drain**

## STYLE 15:
- **PIN 1. Anode**
- **PIN 2. Anode**
- **PIN 3. Anode**
- **PIN 4. Anode**
- **PIN 5. Anode**
- **PIN 6. Anode**
- **PIN 7. Cathode**
- **PIN 8. Cathode**

## STYLE 16:
- **PIN 1. Emitter, Die #1**
- **PIN 2. Anode**
- **PIN 3. Anode**
- **PIN 4. Anode**
- **PIN 5. Anode**
- **PIN 6. Anode**
- **PIN 7. Cathode, Common**
- **PIN 8. Cathode, Common**

## STYLE 17:
- **PIN 1. Vcc**
- **PIN 2. V2out**
- **PIN 3. Vout**
- **PIN 4. Txe**
- **PIN 5. Rxe**
- **PIN 6. Vee**
- **PIN 7. Gnd**
- **PIN 8. Acc**

## STYLE 18:
- **PIN 1. Anode**
- **PIN 2. Anode**
- **PIN 3. Anode**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Cathode**
- **PIN 8. Cathode**

## STYLE 19:
- **PIN 1. Source**
- **PIN 2. Source**
- **PIN 3. Source**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Mirror 2**
- **PIN 8. Mirror 1**

## STYLE 20:
- **PIN 1. Source (N)**
- **PIN 2. Gate**
- **PIN 3. Gate**
- **PIN 4. Gate**
- **PIN 5. Drain**
- **PIN 6. Drain**
- **PIN 7. Drain**
- **PIN 8. Drain**

## STYLE 21:
- **PIN 1. Cathode 1**
- **PIN 2. Cathode 2**
- **PIN 3. Cathode 3**
- **PIN 4. Cathode 4**
- **PIN 5. Cathode 5**
- **PIN 6. Common Anode**
- **PIN 7. Common Anode**
- **PIN 8. Cathode 6**

## STYLE 22:
- **PIN 1. Line 1 IN**
- **PIN 2. Common Cathode/VCC**
- **PIN 3. Common Cathode/VCC**
- **PIN 4. Line 2 IN**
- **PIN 5. Common Anode/Gnd**
- **PIN 6. Common Anode/Gnd**
- **PIN 7. Common Anode/Gnd**
- **PIN 8. Common Anode/Gnd**

## STYLE 23:
- **PIN 1. Base**
- **PIN 2. Common Anode/Gnd**
- **PIN 3. Common Anode/Gnd**
- **PIN 4. Line 2 OUT**
- **PIN 5. Common Anode/Gnd**
- **PIN 6. Common Anode/Gnd**
- **PIN 7. Common Anode/Gnd**
- **PIN 8. Common Anode/Gnd**

## STYLE 24:
- **PIN 1. Base**
- **PIN 2. Emitter**
- **PIN 3. Collector/Anode**
- **PIN 4. Collector/Anode**
- **PIN 5. Cathode**
- **PIN 6. Cathode**
- **PIN 7. Collector/Anode**
- **PIN 8. Collector/Anode**

## STYLE 25:
- **PIN 1. Vin**
- **PIN 2. N/C**
- **PIN 3. Rext**
- **PIN 4. Gnd**
- **PIN 5. Iout**
- **PIN 6. Iout**
- **PIN 7. Iout**
- **PIN 8. Iout**

## STYLE 26:
- **PIN 1. Gnd**
- **PIN 2. Dvdr**
- **PIN 3. Enable**
- **PIN 4. Ilimit**
- **PIN 5. Source**
- **PIN 6. Source**
- **PIN 7. Source**
- **PIN 8. Drain**

## STYLE 27:
- **PIN 1. Ilimit**
- **PIN 2. Dvdr**
- **PIN 3. Enable**
- **PIN 4. Input**
- **PIN 5. Source**
- **PIN 6. Source**
- **PIN 7. Source**
- **PIN 8. Drain**

## STYLE 28:
- **PIN 1. Sw_to_gnd**
- **PIN 2. Dasic_off**
- **PIN 3. Dasic_sw_det**
- **PIN 4. Gnd**
- **PIN 5. V_mon**
- **PIN 6. Vbulk**
- **PIN 7. Vbulk**
- **PIN 8. V**
**NOTES:**

2. CONTROLLING DIMENSION MILLIETERS.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 MM IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE WIRE FLASH, PROTRUSION OR GATE BURNS. WIRE FLASH, PROTRUSION, OR GATE BURNS SHALL NOT EXCEED 0.15 MM PER SIDE. DIMENSION "e" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 MM PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

**RECOMMENDED MOUNTING FOOTPRINT**

*For additional information see factory layout planning and mounting technique reference manual, ON-18909-1.

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**GENERIC MARKING DIAGRAM**

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
*= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "*", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**
- PIN 1: SOURCE
- PIN 2: SOURCE
- PIN 3: SOURCE
- PIN 4: GATE
- PIN 5: DRAIN
- PIN 6: DRAIN
- PIN 7: DRAIN
- PIN 8: DRAIN

**STYLE 2:**
- PIN 1: SOURCE 1
- PIN 2: GATE 1
- PIN 3: SOURCE 2
- PIN 4: GATE 2
- PIN 5: DRAIN 2
- PIN 6: DRAIN 2
- PIN 7: DRAIN 1
- PIN 8: DRAIN 1

**STYLE 3:**
- PIN 1: N-SOURCE
- PIN 2: N-GATE
- PIN 3: P-SOURCE
- PIN 4: P-GATE
- PIN 5: P-DRAIN
- PIN 6: P-DRAIN
- PIN 7: N-DRAIN
- PIN 8: N-DRAIN

**PACKAGE DIMENSIONS**

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