

Darlington Complementary Silicon Power Transistors



ON Semiconductor®

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TIP140, TIP141, TIP142, (NPN); TIP145, TIP146, TIP147, (PNP)

Designed for general-purpose amplifier and low frequency switching applications.

Features

- High DC Current Gain –
 $\text{Min } h_{FE} = 1000 @ I_C = 5.0 \text{ A, } V_{CE} = 4 \text{ V}$
- Collector–Emitter Sustaining Voltage – @ 30 mA
 $V_{CEO(sus)} = 60 \text{ Vdc (Min) – TIP140, TIP145}$
 $= 80 \text{ Vdc (Min) – TIP141, TIP146}$
 $= 100 \text{ Vdc (Min) – TIP142, TIP147}$
- Monolithic Construction with Built–In Base–Emitter Shunt Resistor
- These are Pb–Free Devices*

MAXIMUM RATINGS

Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector – Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector – Base Voltage	V_{CB}	60	80	100	Vdc
Emitter – Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous – Peak (Note 1)	I_C	10 15			Adc
Base Current – Continuous	I_B	0.5			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125			W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

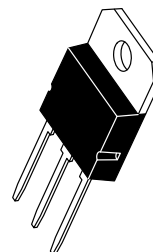
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	35.7	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

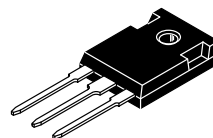
1. 5 ms, $\leq 10\%$ Duty Cycle.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 60–100 VOLTS, 125 WATTS



SOT–93 (TO–218)
CASE 340D
STYLE 1



TO–247
CASE 340L
STYLE 3

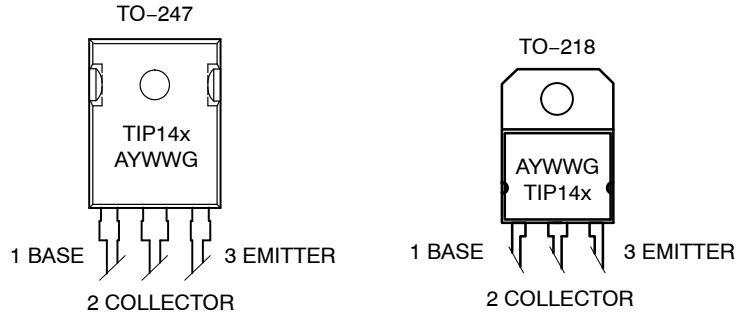
NOTE: Effective June 2012 this device will be available only in the TO–247 package. Reference FPCN# 16827.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

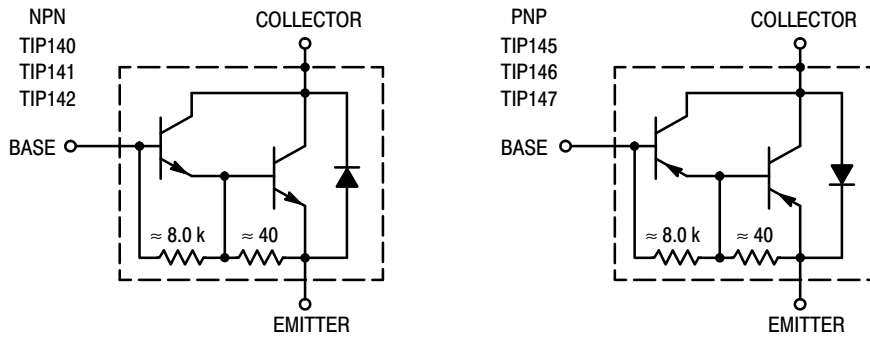
TIP140, TIP141, TIP142, (NPN); TIP145, TIP146, TIP147, (PNP)

MARKING DIAGRAMS



TIP14x = Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

DARLINGTON SCHEMATICS



ORDERING INFORMATION

Device	Package	Shipping
TIP140G	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP141G	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP142G	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP145G	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP146G	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP147G	SOT-93 (TO-218) (Pb-Free)	30 Units / Rail
TIP140G	TO-247 (Pb-Free)	30 Units / Rail
TIP141G	TO-247 (Pb-Free)	30 Units / Rail
TIP142G	TO-247 (Pb-Free)	30 Units / Rail
TIP145G	TO-247 (Pb-Free)	30 Units / Rail
TIP146G	TO-247 (Pb-Free)	30 Units / Rail
TIP147G	TO-247 (Pb-Free)	30 Units / Rail

TIP140, TIP141, TIP142, (NPN); TIP145, TIP146, TIP147, (PNP)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 2) ($I_C = 30\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	60 80 100	– – –	– – –	Vdc
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	I_{CEO}	– – –	– – –	2.0 2.0 2.0	mA
Collector Cutoff Current ($V_{CB} = 60\text{ V}$, $I_E = 0$) ($V_{CB} = 80\text{ V}$, $I_E = 0$) ($V_{CB} = 100\text{ V}$, $I_E = 0$)	I_{CBO}	– – –	– – –	1.0 1.0 1.0	mA
Emitter Cutoff Current ($V_{BE} = 5.0\text{ V}$)	I_{EBO}	–	–	2.0	mA

ON CHARACTERISTICS (Note 2)

DC Current Gain ($I_C = 5.0\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 10\text{ A}$, $V_{CE} = 4.0\text{ V}$)	h_{FE}	1000 500	– –	– –	–
Collector–Emitter Saturation Voltage ($I_C = 5.0\text{ A}$, $I_B = 10\text{ mA}$) ($I_C = 10\text{ A}$, $I_B = 40\text{ mA}$)	$V_{CE(sat)}$	– –	– –	2.0 3.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 10\text{ A}$, $I_B = 40\text{ mA}$)	$V_{BE(sat)}$	–	–	3.5	Vdc
Base–Emitter On Voltage ($I_C = 10\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	–	–	3.0	Vdc

SWITCHING CHARACTERISTICS

Resistive Load (See Figure 1)						
Delay Time	$(V_{CC} = 30\text{ V}$, $I_C = 5.0\text{ A}$, $I_B = 20\text{ mA}$, Duty Cycle $\leq 2.0\%$, $I_{B1} = I_{B2}$, R_C & R_B Varied, $T_J = 25^\circ\text{C}$)	t_d	–	0.15	–	μs
Rise Time		t_r	–	0.55	–	μs
Storage Time		t_s	–	2.5	–	μs
Fall Time		t_f	–	2.5	–	μs

2. Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

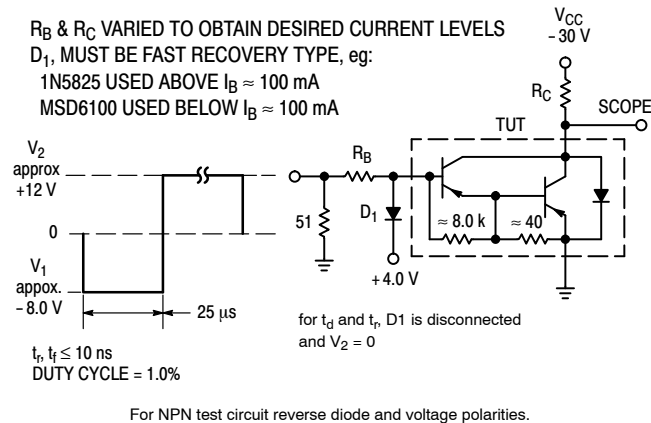


Figure 1. Switching Times Test Circuit

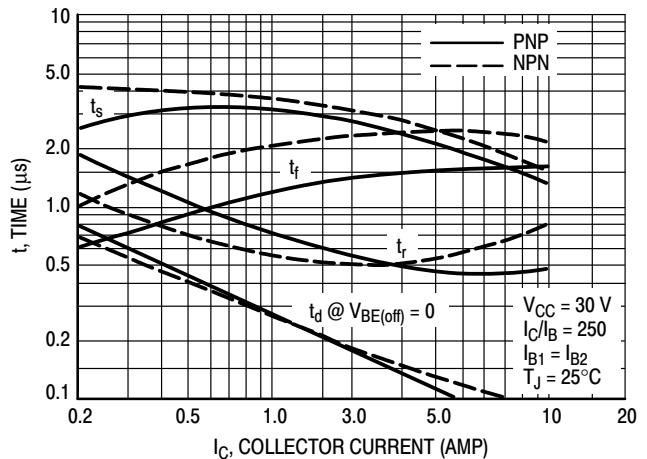


Figure 2. Switching Times

TIP140, TIP141, TIP142, (NPN); TIP145, TIP146, TIP147, (PNP)

TYPICAL CHARACTERISTICS

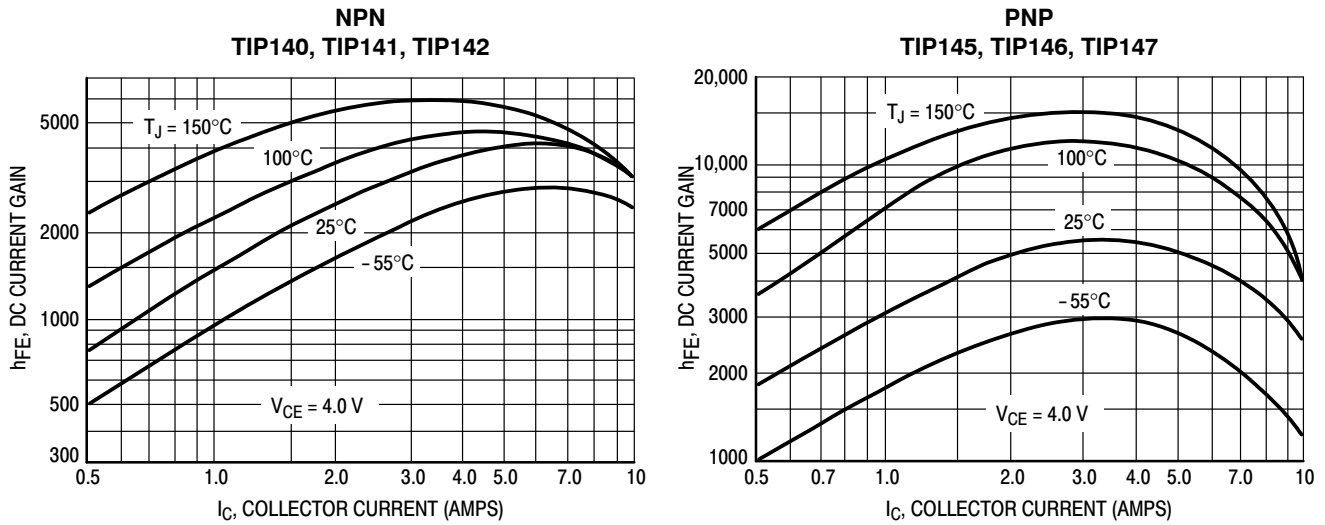


Figure 3. DC Current Gain versus Collector Current

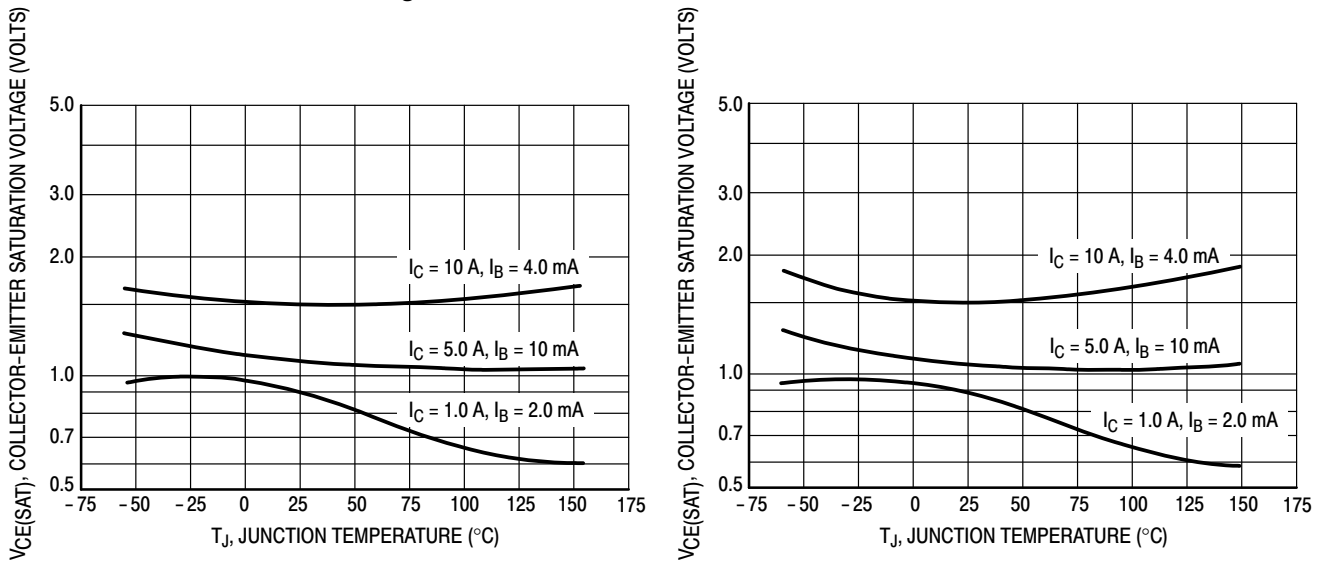


Figure 4. Collector-Emitter Saturation Voltage

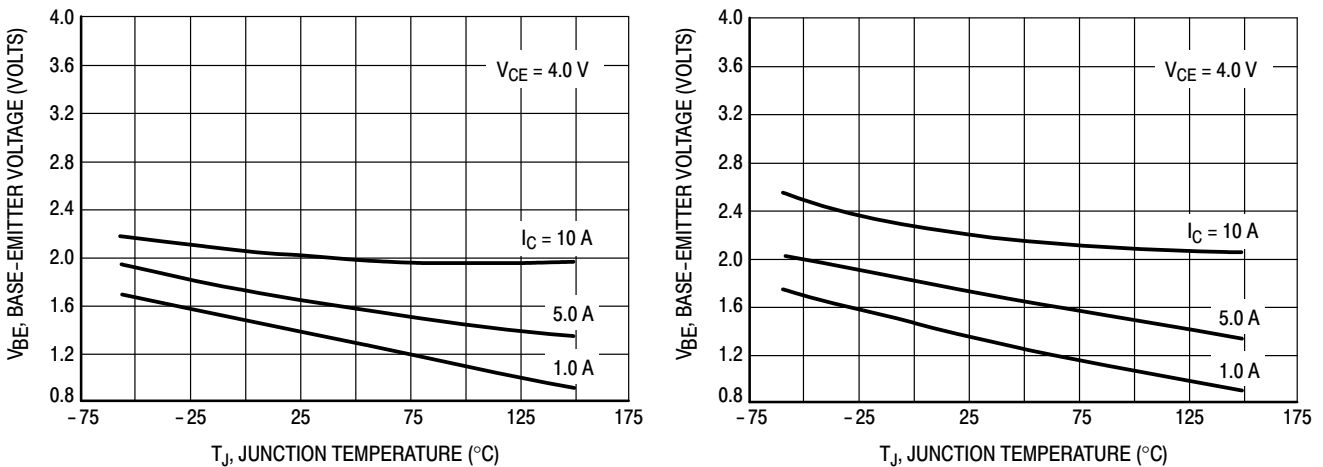


Figure 5. Base-Emitter Voltage

TIP140, TIP141, TIP142, (NPN); TIP145, TIP146, TIP147, (PNP)

ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

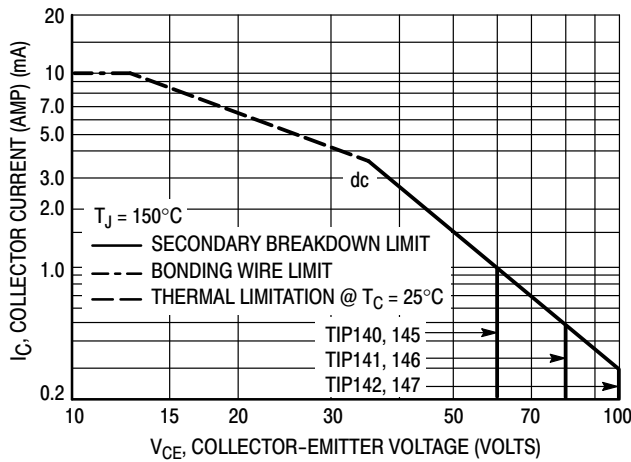


Figure 6. Active-Region Safe Operating Area

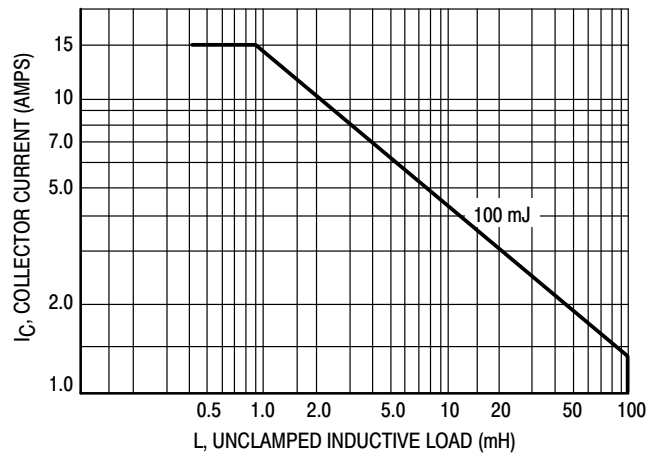
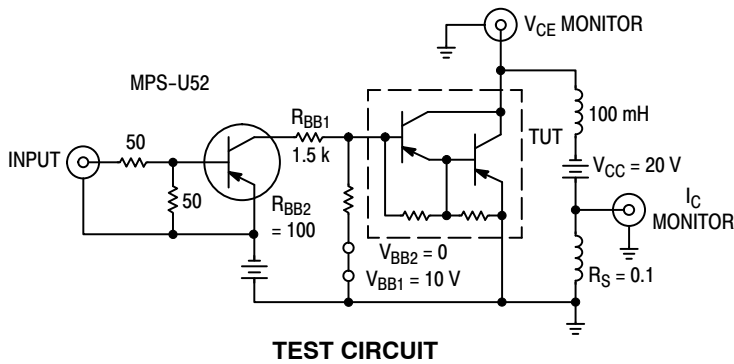
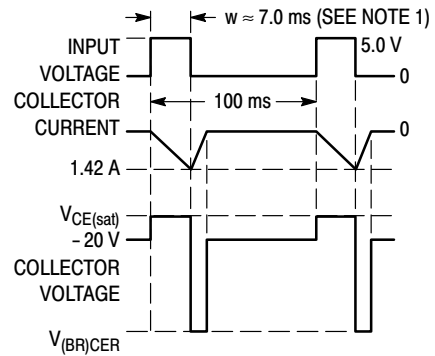


Figure 7. Unclamped Inductive Load



TEST CIRCUIT

NOTE 1: Input pulse width is increased until $I_{CM} = 1.42\text{ A}$.
NOTE 2: For NPN test circuit reverse polarities.



VOLTAGE AND CURRENT WAVEFORMS

Figure 8. Inductive Load

TIP140, TIP141, TIP142, (NPN); TIP145, TIP146, TIP147, (PNP)

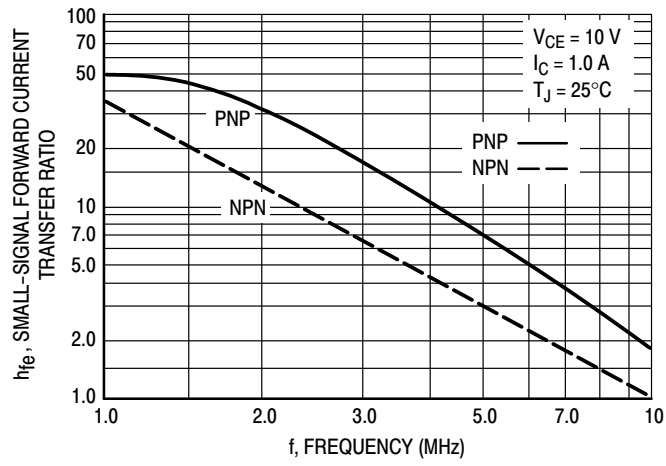


Figure 9. Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio

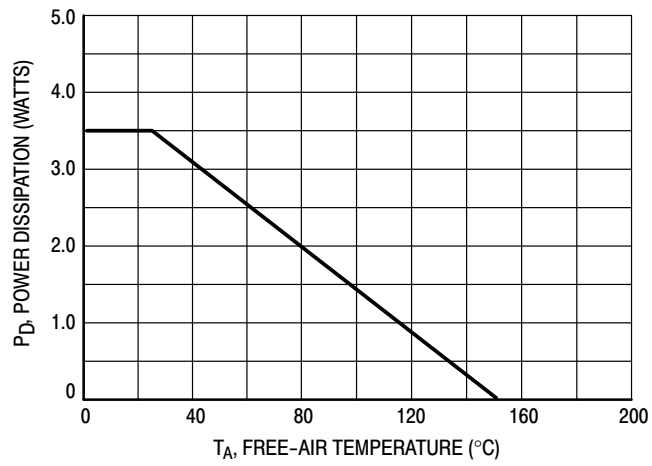


Figure 10. Free-Air Temperature Power Derating

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SOT-93 (TO-218) CASE 340D-02 ISSUE E

DATE 01/03/2002



SCALE 1:1



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

MARKING DIAGRAM

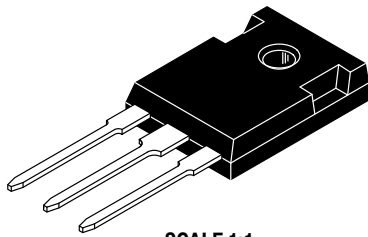


A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

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DESCRIPTION:	SOT-93	PAGE 1 OF 1

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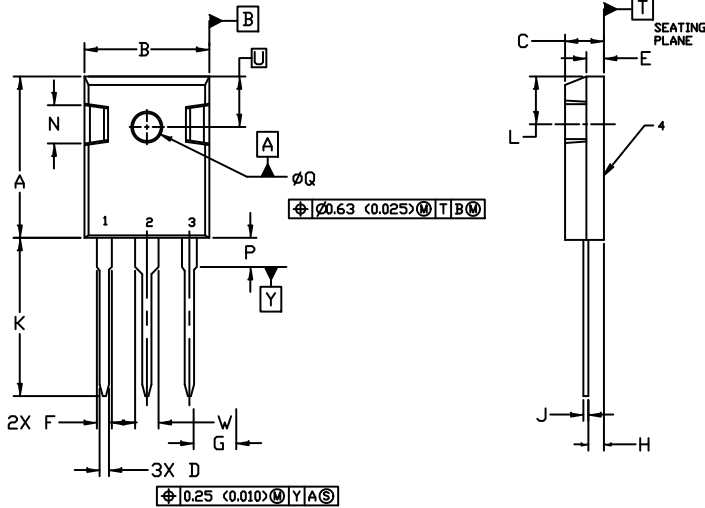
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TO-247
CASE 340L
ISSUE G

DATE 06 OCT 2021

SCALE 1:1

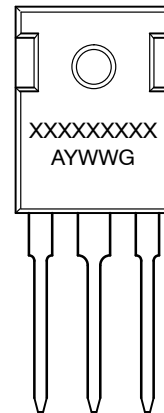


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	----	4.50	----	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

GENERIC
MARKING DIAGRAM*



- | | | | |
|--|--|--|--|
| <p>STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)</p> | <p>STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> |
| <p>STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2</p> | | |

- XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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