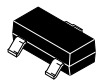
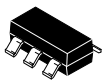
ESD Protection Diode

Low Clamping Voltage

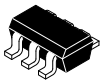
PACDN042



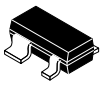
SOT−23-3
CASE 318



SOT-23-5
CASE 527AH



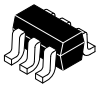
SOT-23-6
CASE 527AJ



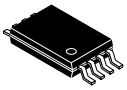
SOT-143
CASE 527AF

SC70-3
CASE 419AB

CS70-5
CASE 419AC



SC70-6
CASE 419AD



TSSOP8
CASE 948AL

MSOP8
CASE 846AB

Product Description

The PACDN042/43/44/45/46 family of surge protection arrays provide a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The PACDN042/43/44/45/46 devices safely dissipate ESD strikes, exceeding the IEC 61000-4-2 International Standard, Level 4 (±8 kV contact discharge). All pins are rated to withstand ±20 kV ESD pulses using the IEC 61000-4-2 contact discharge method. Using the MIL-STD-883D (Method 3015) specification for Human Body Model (HBM) ESD, all pins are protected from contact discharges of greater than ±30 kV.

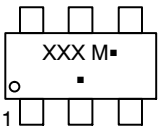
Features

- Two, Three, Four, Five, or Six Surge Protection
- Compact SMT Package Saves Board Space and Facilitates Layout in Space-Critical Applications
- In-System ESD Protection to ±20 kV Contact Discharge, per the IEC 61000-4-2 International Standard
- These Devices are Pb-Free and are RoHS Compliant

Applications

- ESD Protection of PC Ports, Including USB Ports, Serial Ports, Parallel Ports, IEEE1394 Ports, Docking Ports, Proprietary Ports, etc.
- Protection of Interface Ports or IC Pins which are Exposed to High ESD Levels

MARKING DIAGRAM



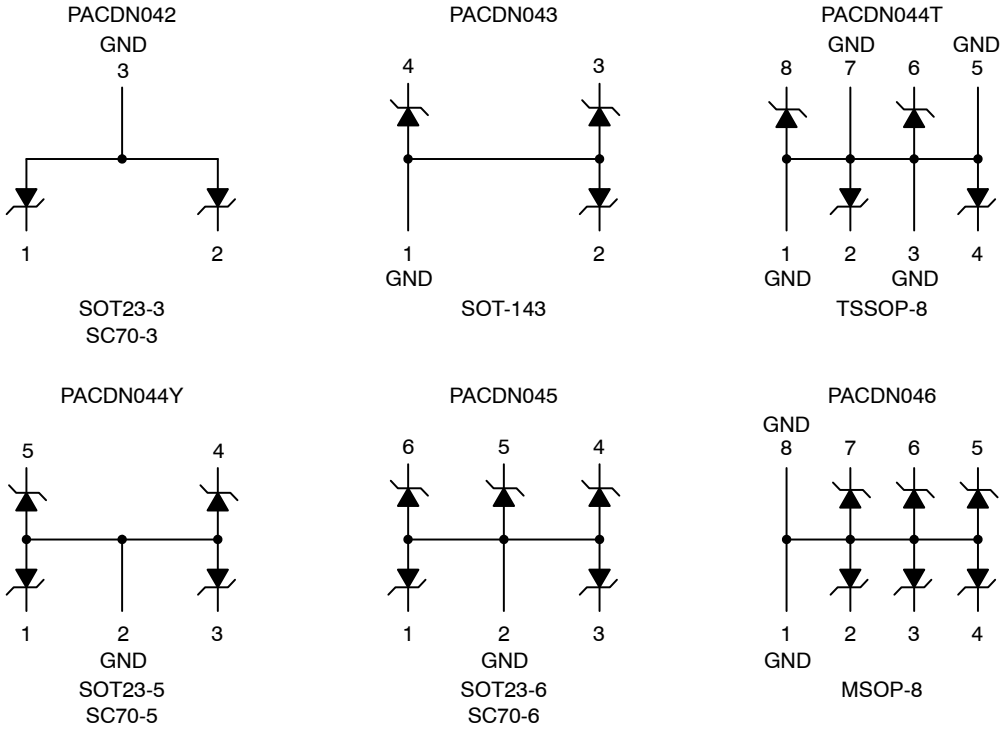
XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

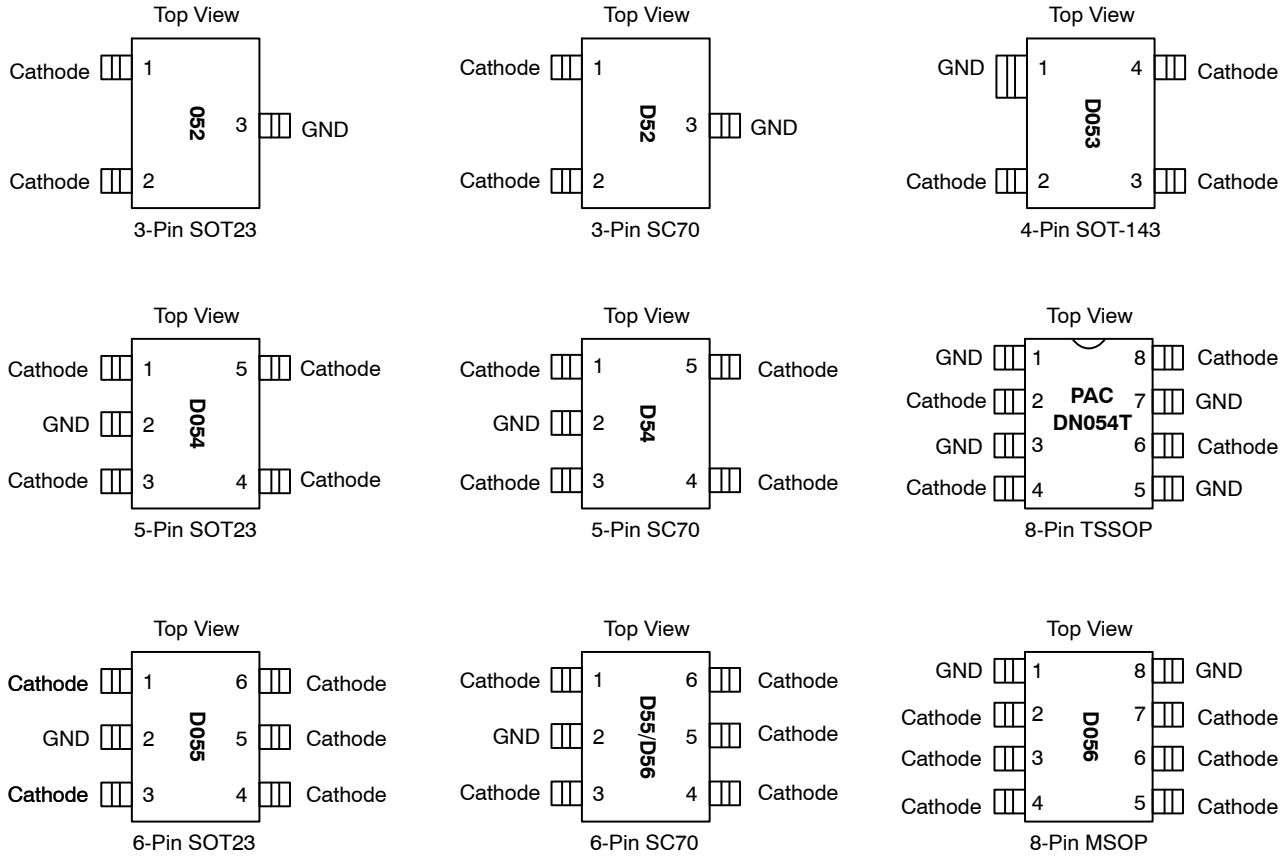
See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAMS



Note: SOT23, SC70, SOT-143, TSSOP, and MSOP Packages may differ in size. These drawings are not to scale.

Table 1. PIN DESCRIPTIONS

Pins	Name	Description
(Refer to Package Outline Drawings)	Cathode	The cathode of the respective surge protection diode, which should be connected to the node requiring transient voltage protection.
(Refer to Package Outline Drawings)	GND	The anode of the surge protection diodes.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Storage Temperature Range	−65 to +150	°C
Package Power Dissipation SC70 SOT23-3, SOT23-5, SOT23-6, SOT-143 TSSOP, MSOP	 0.2 0.225 0.5	W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Unit
Operating Temperature	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C	Capacitance	T_A = 25 °C, 2.5 VDC, 1 MHz		30		pF
V_{RSO}	Reverse Stand-off Voltage	I_R = 10 μA, T_A = 25 °C	5.5			V
		I_R = 1 mA, T_A = 25 °C	6.1			V
I_{LEAK}	Leakage Current	V_{IN} = 5.0 VDC, T_A = 25 °C		1	100	nA
V_{SIG}	Small Signal Clamp Voltage Positive Clamp Negative Clamp	 I = 10 mA, T_A = 25 °C I = −10 mA, T_A = 25 °C	 6.2 −0.4	 6.8 −0.8	 8 −1.2	V
V_{ESD}	ESD Withstand Voltage Human Body Model, MIL-STD-883, Method 3015 Contact Discharge per IEC 61000-4-2 Standard	 (Note 1) (Note 1)	 ±30 ±20			kV
R_D	Diode Dynamic Resistance Forward Conduction Reverse Conduction			 1.0 1.4		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ESD voltage applied between channel pins & ground, one pin at a time; all other channel pins open; all GND pins grounded.

PERFORMANCE INFORMATION

Diode Capacitance

Typical diode capacitance with respect to positive cathode voltage (reverse voltage across the diode) is given in Diode Capacitance vs. Reverse Voltage.

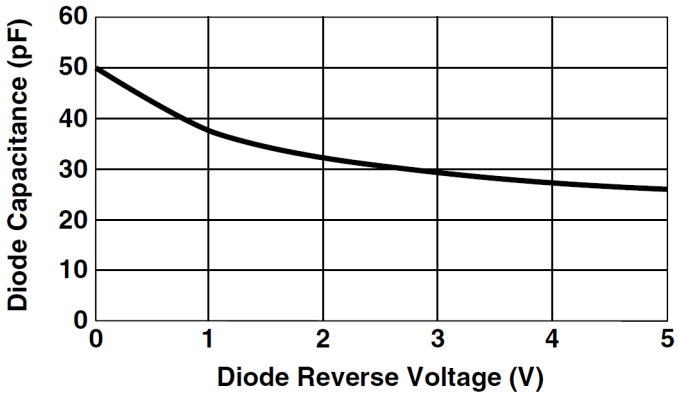


Figure 1. Diode Capacitance vs. Reverse Voltage

Typical High Current Diode Characteristics

Measurements are made in pulse mode with a nominal pulse width of 0.7 mS.

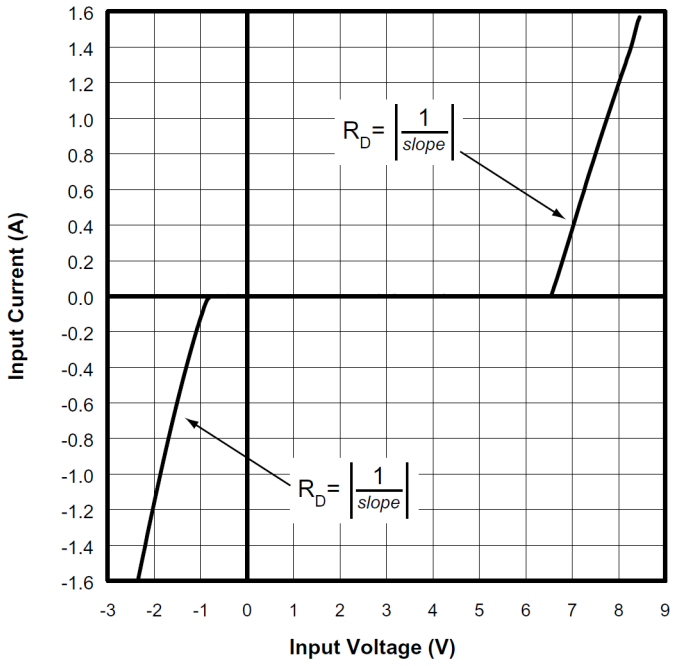


Figure 2. Typical Input VI Characteristics
(Pulse-mode measurements, pulse width = 0.7 mS nominal)

ORDERING INFORMATION

Device	Package	Shipping†
PACDN042Y3R	SOT23-3 (Pb-Free)	3000 / Tape & Reel
PACDN045YB6R-R	SC70-6 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 2)

PACDN044Y5R	SOT23-5 (Pb-Free)	3000 / Tape & Reel
PACDN045Y6R	SOT23-6 (Pb-Free)	3000 / Tape & Reel
PACDN043Y4R	SOT-143 (Pb-Free)	3000 / Tape & Reel
PACDN042YB3R	SC70-3 (Pb-Free)	3000 / Tape & Reel
PACDN044YB5R	SC70-5 (Pb-Free)	3000 / Tape & Reel
PACDN045YB6R	SC70-6 (Pb-Free)	3000 / Tape & Reel
PACDN044TR	TSSOP8 (Pb-Free)	2500 / Tape & Reel
PACDN046MR	MSOP8 (Pb-Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

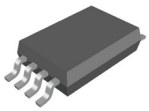
2. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

REVISION HISTORY

Revision	Description of Changes	Date
9	Rebranded the Data Sheet to **onsemi** format. PACDN044Y5R, PACDN045Y6R, PACDN043Y4R, PACDN042YB3R, PACDN044YB5R, PACDN045YB6R, PACDN044TR, PACDN046MR OPNs Marked as Discontinued.	09/10/2025

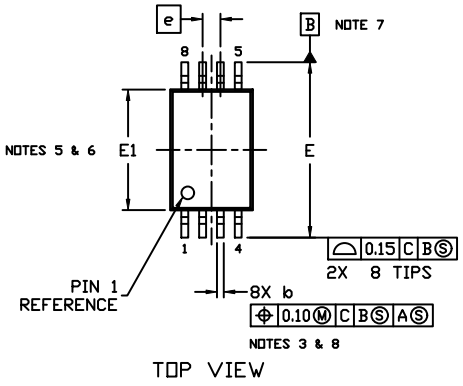
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

PACKAGE DIMENSIONS

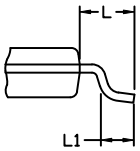


TSSOP8, 4.4x3.0, 0.65P
CASE 948AL
ISSUE A

DATE 20 MAY 2022



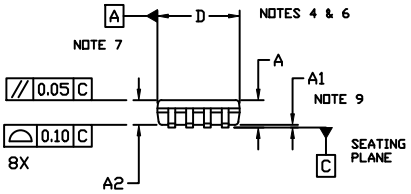
TOP VIEW



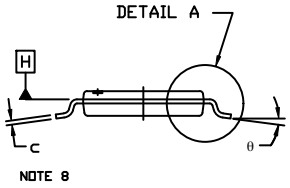
DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009..
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP..
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY..



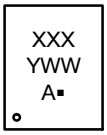
SIDE VIEW



END VIEW

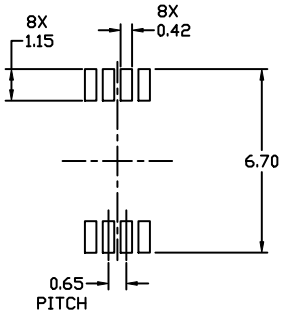
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC MARKING DIAGRAM*



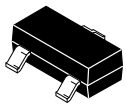
XXX = Specific Device Code
Y = Year
WW = Work Week
A = Assembly Location
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT*

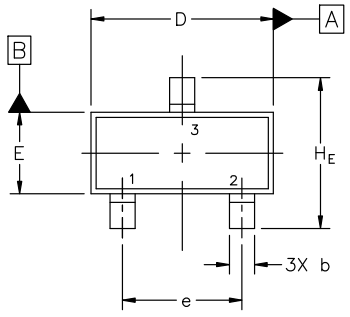
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



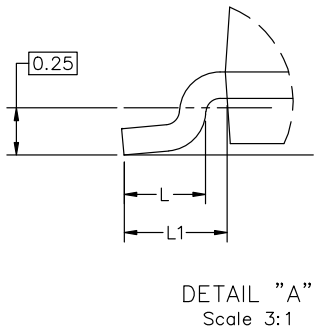
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

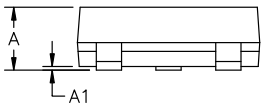
DATE 14 AUG 2024



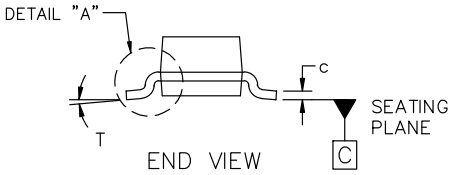
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

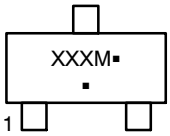


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

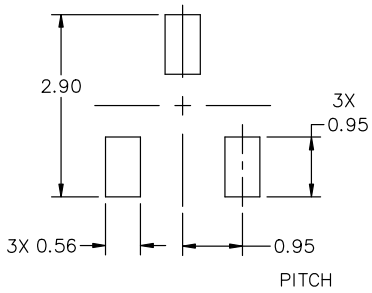
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

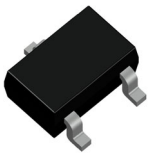
STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

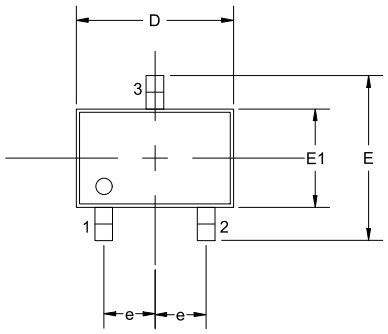
STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

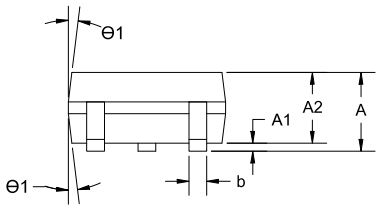


SC−70, 3 Lead, 1.25x2
CASE 419AB
ISSUE A

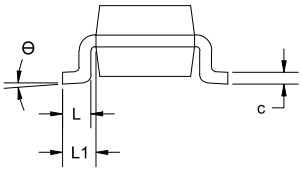
DATE 13 FEB 2023



TOP VIEW



SIDE VIEW

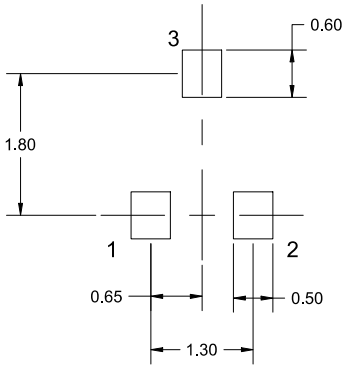


END VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. COMPLIES WITH JEDEC MO-203

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80		1.10
A1	0.00		0.10
A2	0.80	0.90	1.00
b	0.15		0.30
c	0.08		0.22
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
Θ	0°		8°
Θ1	4°		10°



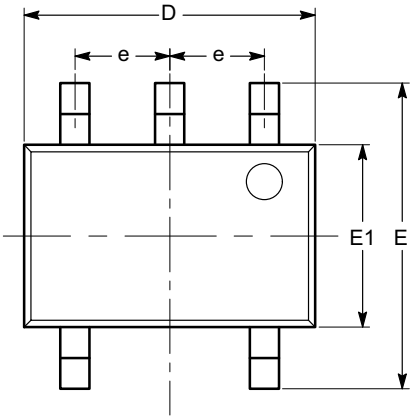
SOLDERING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON34256E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SC−70, 3 LEAD, 1.25X2**	**PAGE 1 OF 1**

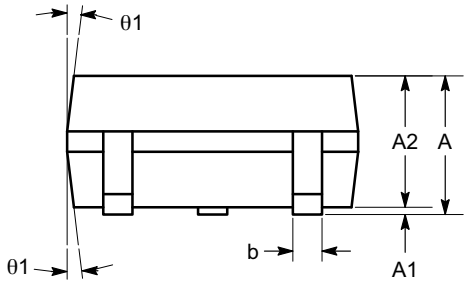
SC−88A (SC−70 5 Lead), 1.25x2
CASE 419AC−01
ISSUE A

DATE 29 JUN 2010

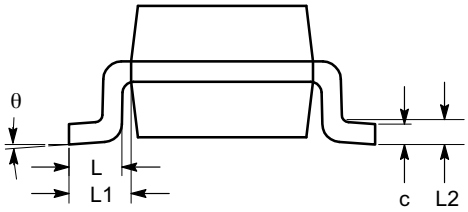


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



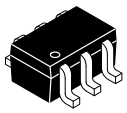
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

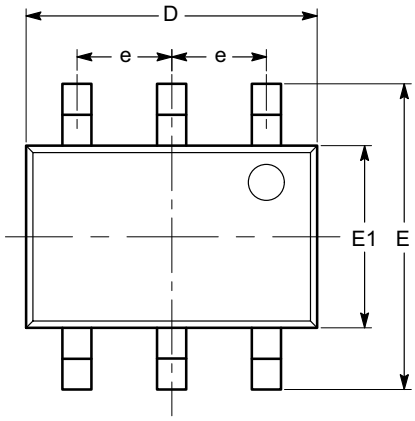
DOCUMENT NUMBER:	98AON34260E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC−88A (SC−70 5 LEAD), 1.25X2	PAGE 1 OF 1



1

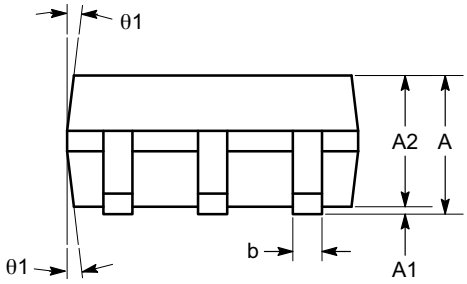
SC−88 (SC−70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

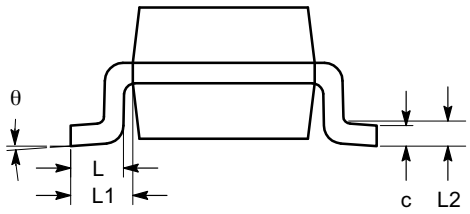


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



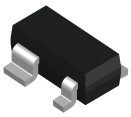
SIDE VIEW



END VIEW

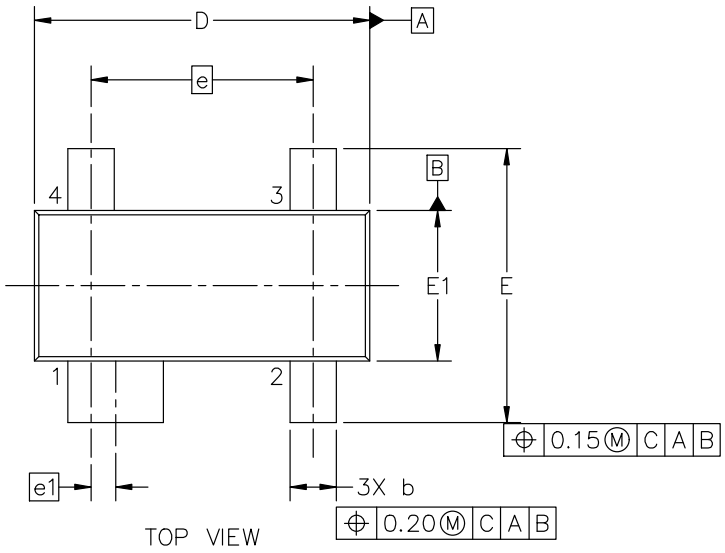
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

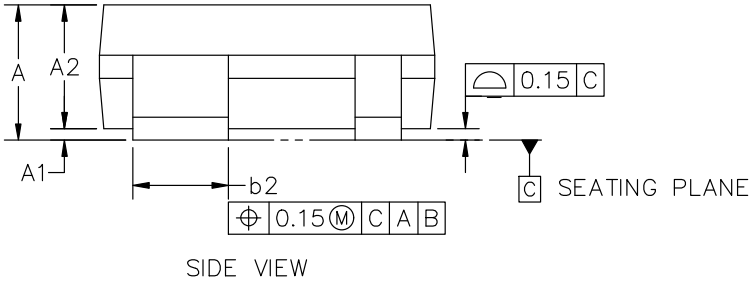
DOCUMENT NUMBER:	**98AON34266E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SC−88 (SC−70 6 LEAD), 1.25X2**	**PAGE 1 OF 1**

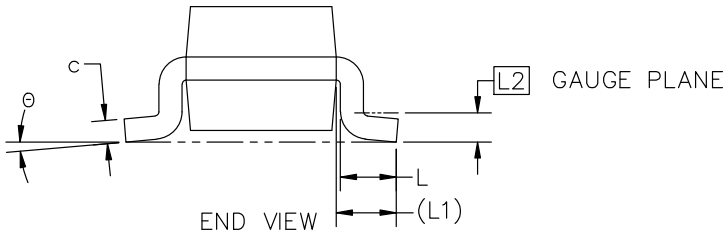


SOT−143, 4 LEAD, 2.90x1.30x0.90, 1.92P
CASE 527AF
ISSUE B

DATE 26 FEB 2024





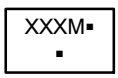


NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5M, 2018
2. CONTROLLING DIMENSION: MILLIMETERS

SYMBOL	MIN	NOM	MAX
A	0.80	1.01	1.22
A1	0.05	0.10	0.15
A2	0.75	0.90	1.07
b	0.30	0.40	0.50
b2	0.76	0.83	0.89
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	2.10	2.37	2.64
E1	1.20	1.30	1.40
e	1.92 BSC		
e1	0.20 BSC		
L	0.40	0.50	0.60
L1	0.54 REF		
L2	0.25 BSC		
θ	0°	–	8°

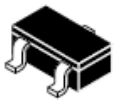
GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

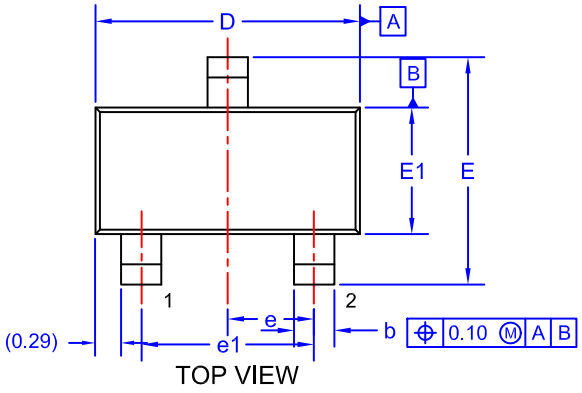
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON34306E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−143, 4 LEAD, 2.90x1.30x0.90, 1.92P**	**PAGE 1 OF 1**



SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019

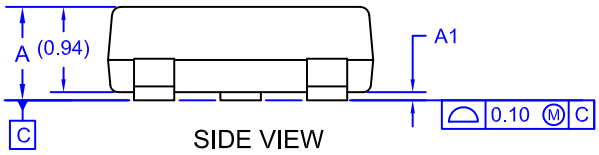


TOP VIEW

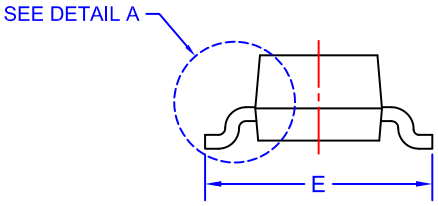
NOTES: UNLESS OTHERWISE SPECIFIED

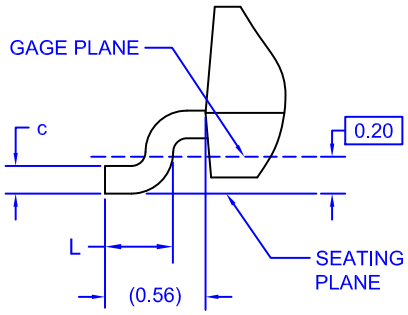
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43

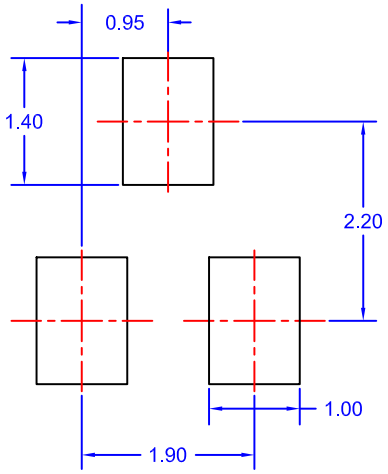


SIDE VIEW





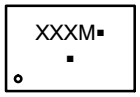
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

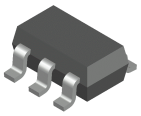


XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

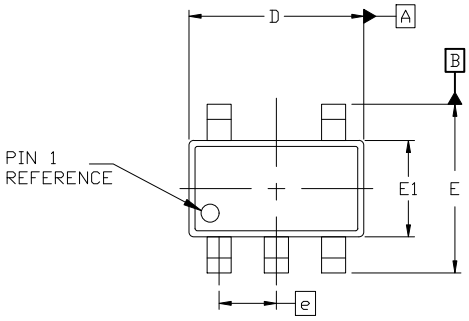
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

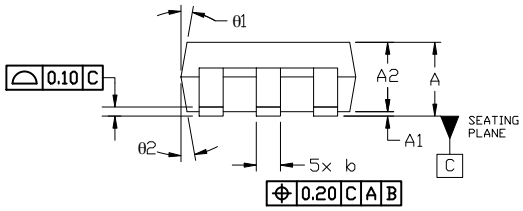
DOCUMENT NUMBER:	**98AON34319E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−23/SUPERSOT−23, 3 LEAD, 1.4X2.9**	**PAGE 1 OF 1**

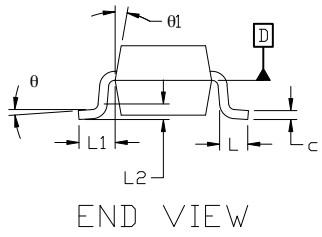


SOT−23, 5 Lead
CASE 527AH
ISSUE A

DATE 09 JUN 2021



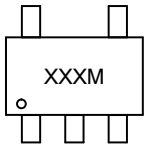




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

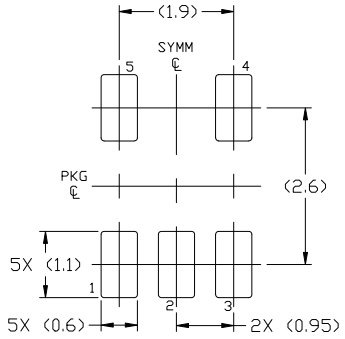
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

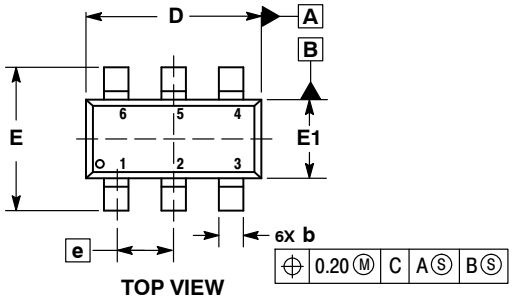
For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

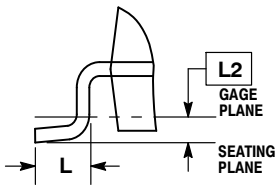
DOCUMENT NUMBER:	**98AON34320E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23, 5 LEAD**		**PAGE 1 OF 1**

SOT−23, 6 Lead
CASE 527AJ
ISSUE B

DATE 29 FEB 2012

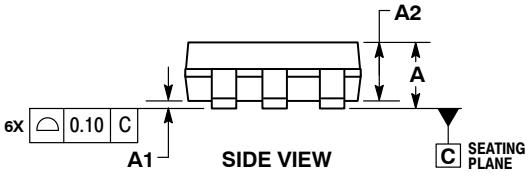
SCALE 2:1

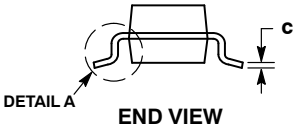




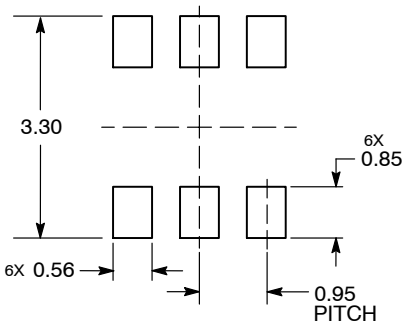
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	





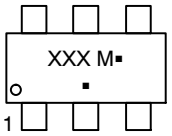
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

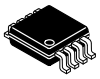


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

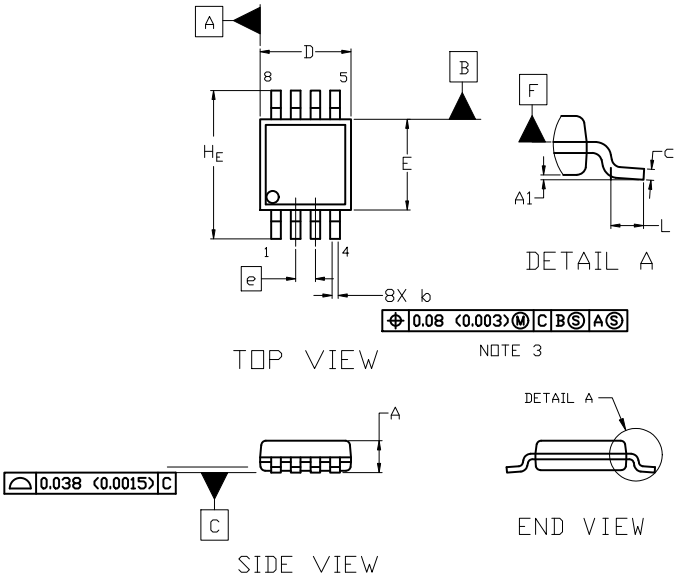
DOCUMENT NUMBER:	**98AON34321E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−23, 6 LEAD**	**PAGE 1 OF 1**



SCALE 2:1

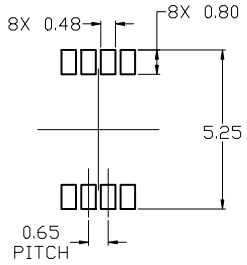
Micro8
CASE 846A−02
ISSUE K

DATE 16 JUL 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

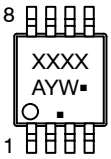


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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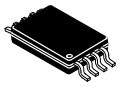
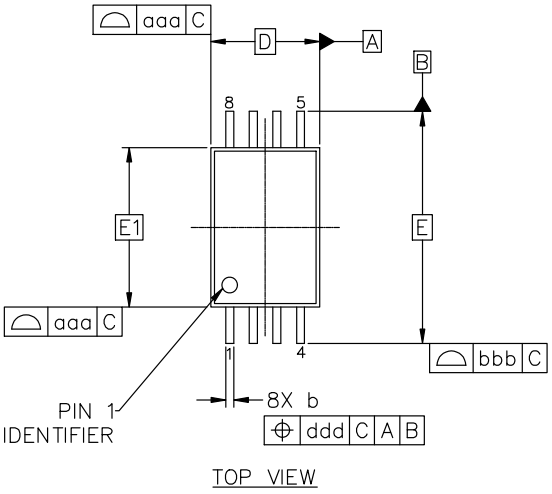
DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**



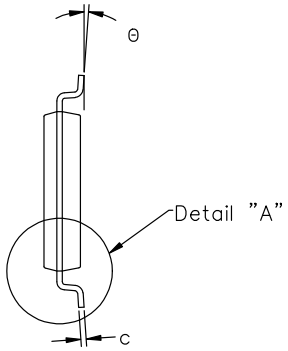
SCALE 2:1

TSSOP−8 3.00x4.00x0.90, 0.65P
CASE 948S
ISSUE D

DATE 24 OCT 2025

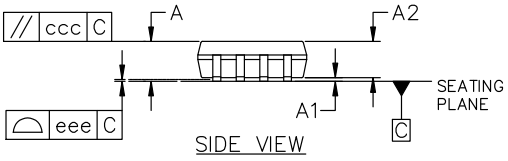


TOP VIEW

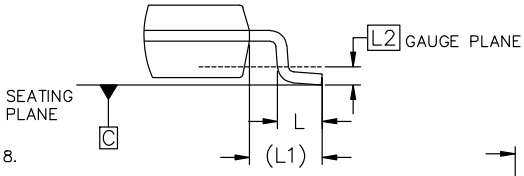


FRONT VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.05	0.10	0.15
A2	0.80	0.90	1.00
b	0.19	0.25	0.30
c	0.09	0.15	0.20
D	3.00 BSC		
E	6.40 BSC		
E1	4.40 BSC		
L	0.50	0.60	0.70
L1	1.00 REF		
L2	0.25 BSC		
θ	0°	4°	8°
TOLERANCE FORM & POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.10		
eee	0.05		

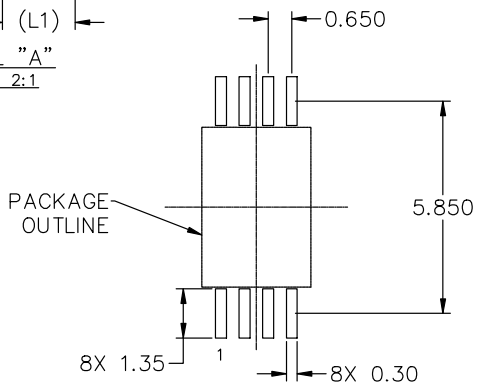


SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07mm.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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