

MOSFET - Power, N-Channel, Shielded Gate 80 V, 8.3 mΩ, 61 A

NVTF8D1N08H

Features

- Small Footprint (3x3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVTF8D1N08H – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

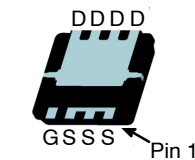
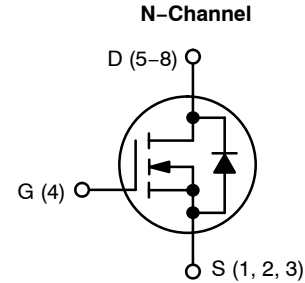
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DS}	80	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	61	A
		$T_C = 100^\circ\text{C}$		43	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D	75	W
		$T_C = 100^\circ\text{C}$		38	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	14	A
		$T_A = 25^\circ\text{C}$		10	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	3.8	W
		$T_A = 25^\circ\text{C}$		1.9	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 100 \mu\text{s}$	I_{DM}	216	A	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	61	A	
Single Pulse Drain-to-Source Avalanche Energy		E_{AS}	113	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

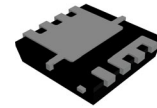
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
80 V	8.3 mΩ @ 10 V	61 A

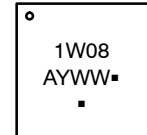
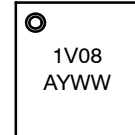


WDFN8
(3.3x3.3, 0.65 P)
CASE 511DY



WDFNW8
(3.3x3.3, 0.65 P)
CASE 515AP

MARKING DIAGRAMS



1V08/1W08 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package
(Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVTFS8D1N08H

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 4)	$R_{\theta JC}$	2	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	39	

4. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80	-	-	V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		-	52	-	mV/°C	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 64\text{ V}$	$T_J = 25^\circ\text{C}$	-	-	10	μA
			$T_J = 125^\circ\text{C}$	-	-	250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$	-	-	100	nA	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 270\ \mu\text{A}$	2.0	2.8	4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$		-	-7.2	-	mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 16\text{ A}$	-	6.4	8.3	m Ω
		$V_{GS} = 6\text{ V}, I_D = 13\text{ A}$	-	9	12.6	

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$	-	1450	-	μF
Output Capacitance	C_{OSS}		-	776	-	
Reverse Transfer Capacitance	C_{RSS}		-	46	-	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 40\text{ V}; I_D = 16\text{ A}$	-	9	-	nC
		$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 16\text{ A}$	-	23	-	
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 16\text{ A}$	-	9	-	nC
Gate-to-Source Charge	Q_{GS}		-	7.2	-	
Gate-to-Drain Charge	Q_{GD}		-	4.2	-	
Plateau Voltage	V_{GP}		-	4.6	-	

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}, I_D = 16\text{ A}, R_G = 2.5\ \Omega$	-	9.1	-	ns
Rise Time	t_r		-	13	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	23.8	-	
Fall Time	t_f		-	2.5	-	

DRAIN-SOURCE DIODE CHARACTERISTICS

Source-to-Drain Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$	-	0.81	1.2	V
Reverse Recovery Time	t_{RR}	$I_F = 16\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	40.5	-	ns
Reverse Recovery Charge	Q_{RR}		-	46.8	-	nC
Charge Time	t_a		-	22.6	-	ns
Discharge Time	t_b		-	17.9	-	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

NVTFS8D1N08H

TYPICAL CHARACTERISTICS

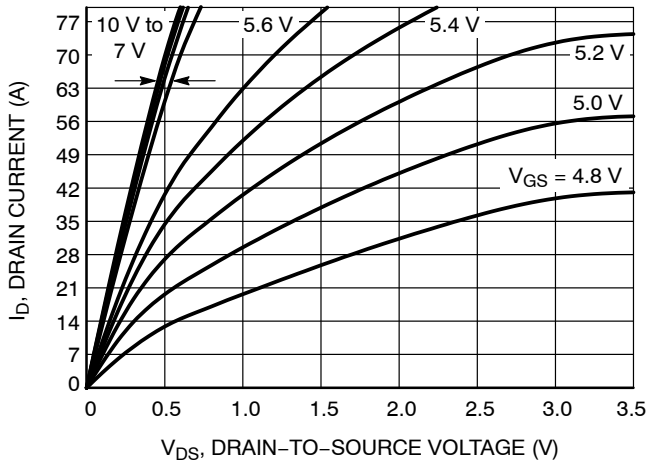


Figure 1. On-Region Characteristics

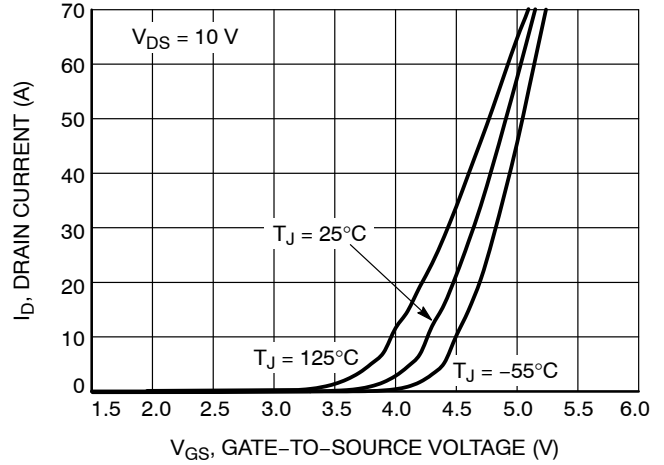


Figure 2. Transfer Characteristics

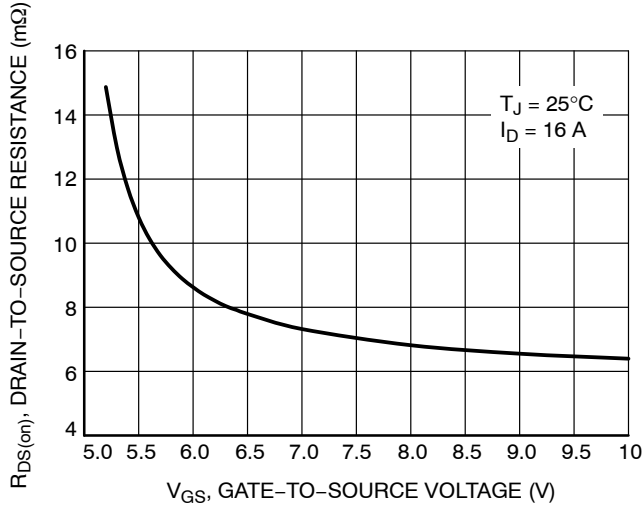


Figure 3. On-Resistance vs. Gate-to-Source Voltage

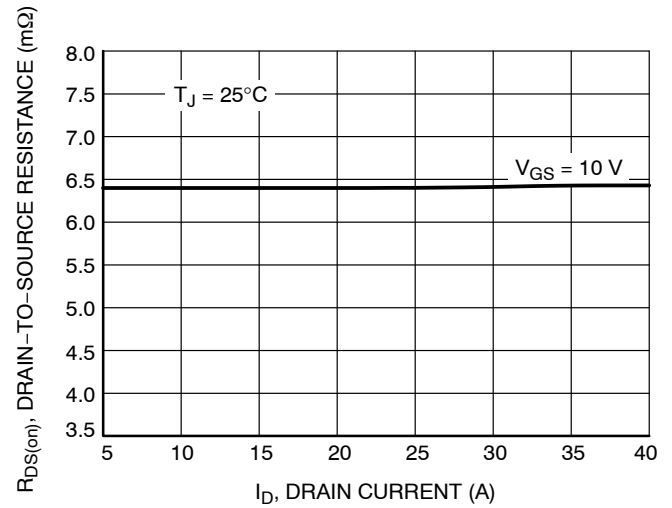


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

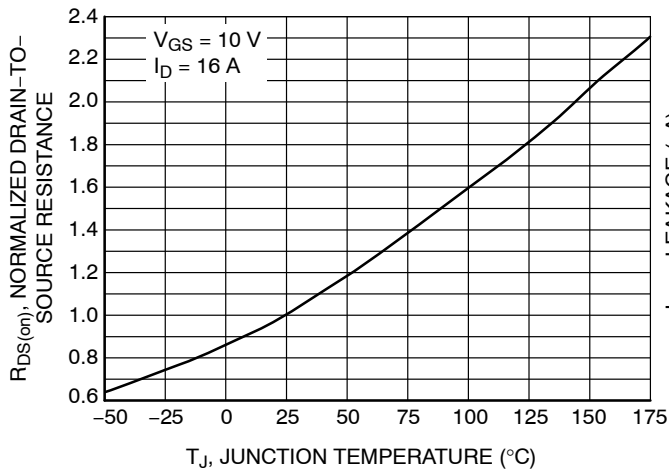


Figure 5. On-Resistance Variation with Temperature

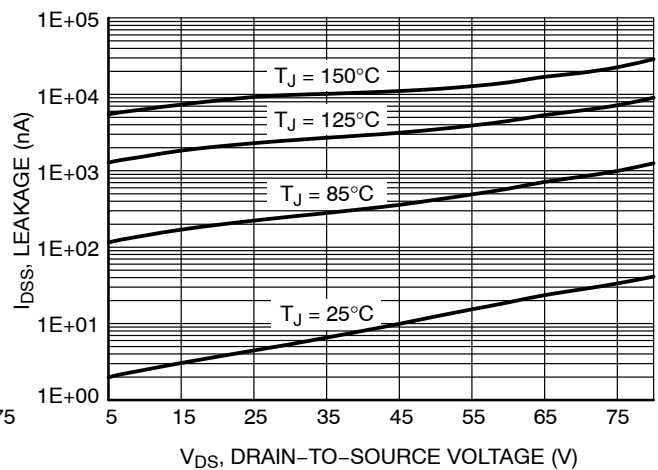


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVTFS8D1N08H

TYPICAL CHARACTERISTICS

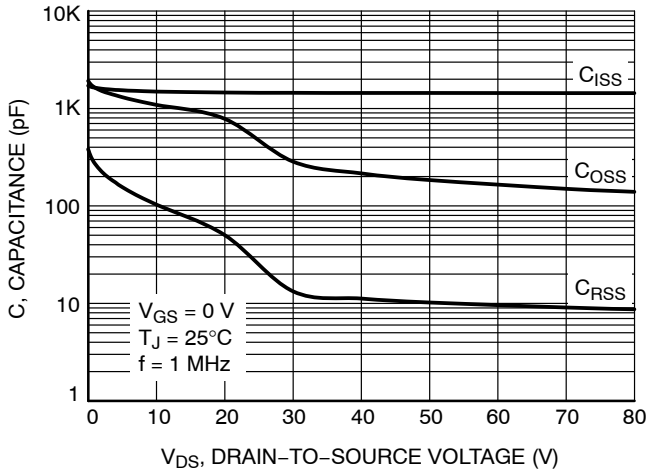


Figure 7. Capacitance Variation

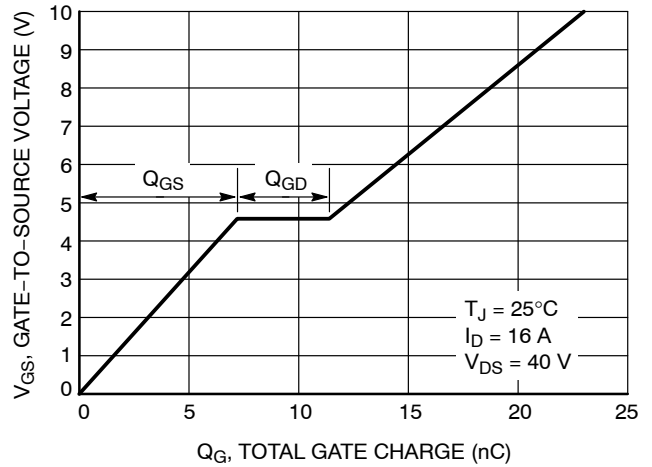


Figure 8. Gate-to-Source Voltage vs. Total Charge

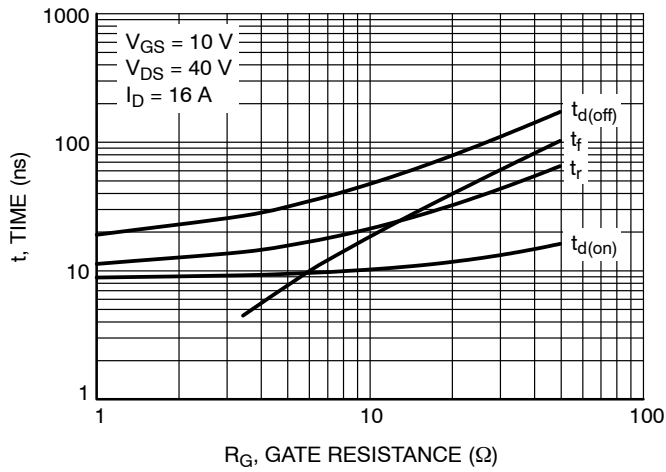


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

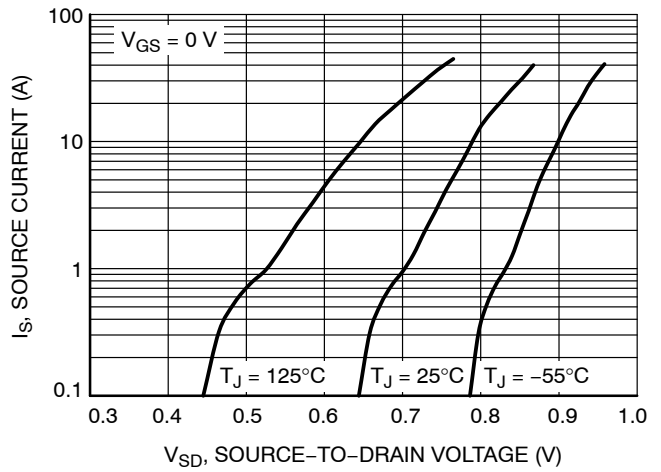


Figure 10. Diode Forward Voltage vs. Current

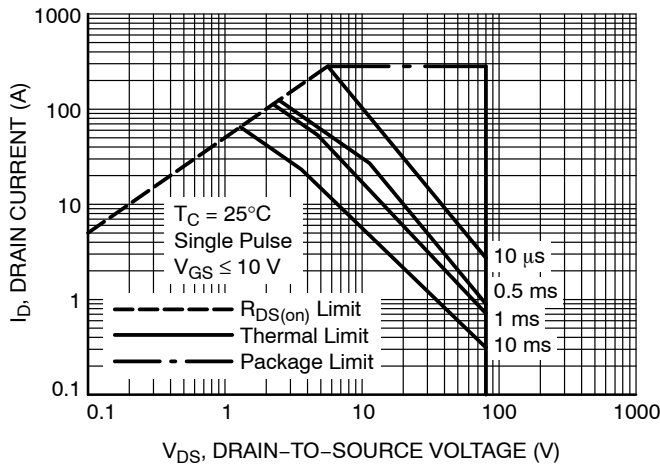


Figure 11. Maximum Rated Forward Biased Safe Operating Area

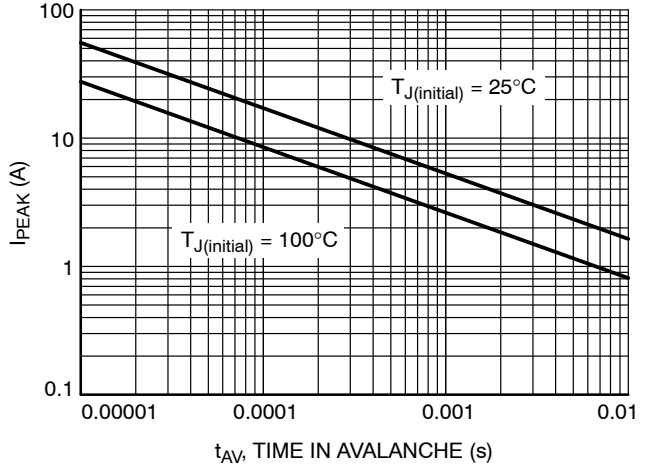


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVTFS8D1N08H

TYPICAL CHARACTERISTICS

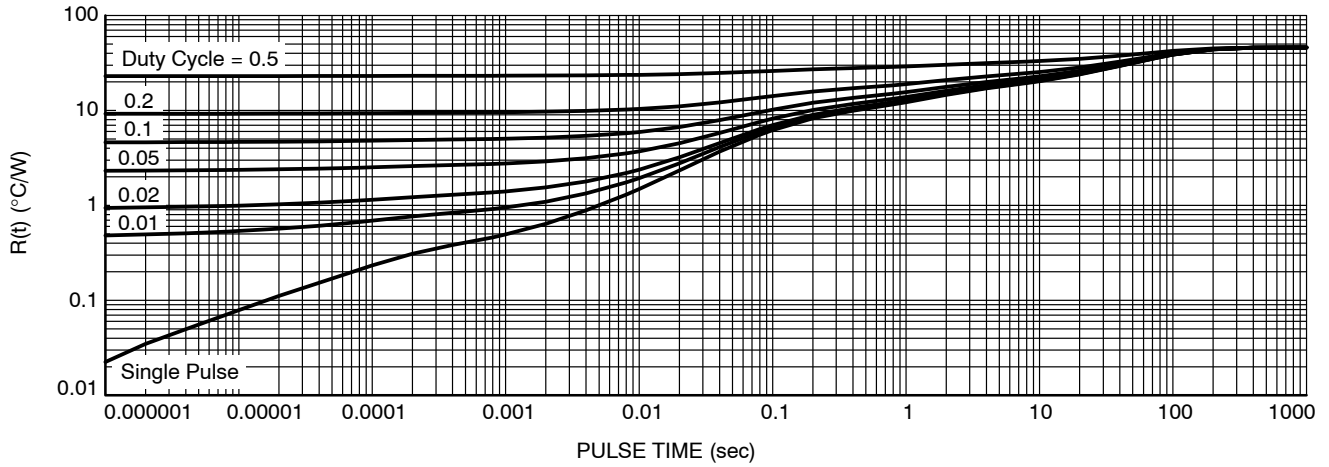


Figure 13. Transient Thermal Impedance

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVTFS8D1N08HTAG	1V08	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFWS8D1N08HTAG	1W08	WDFNW8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

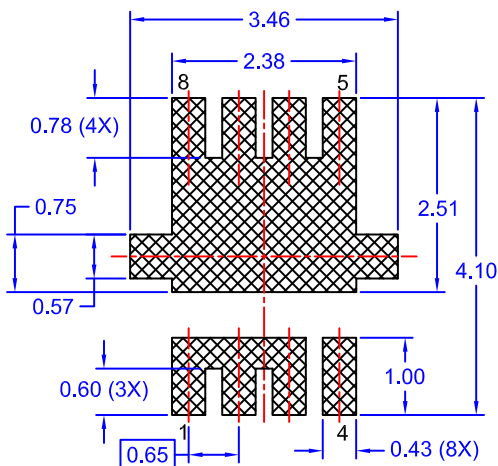
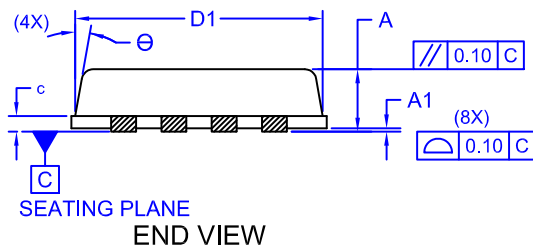
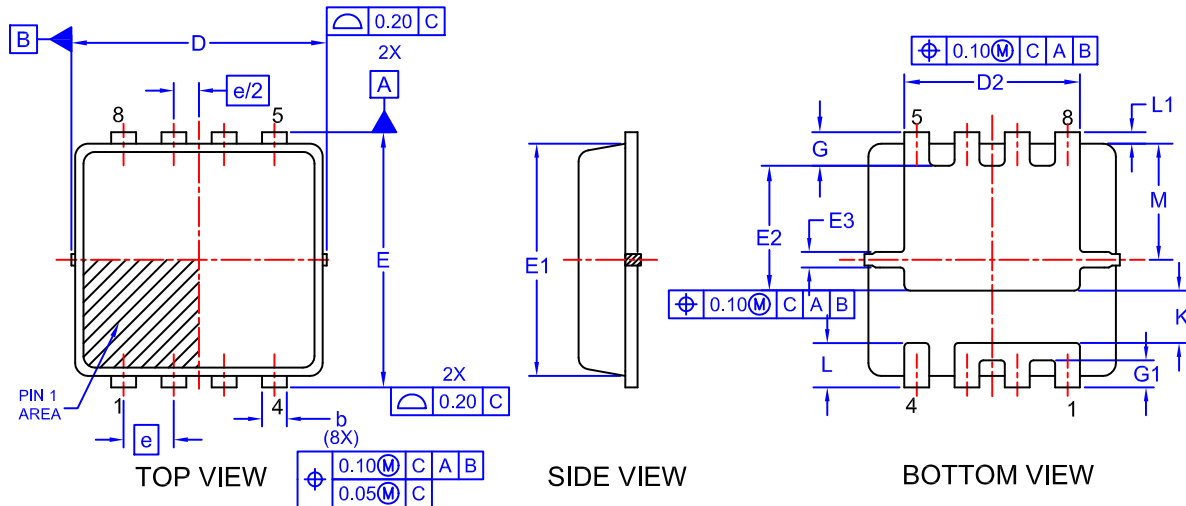
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



WDFN8 3.3x3.3, 0.65P
CASE 511DY
ISSUE A

DATE 21 AUG 2018



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
Θ	0	-	12

GENERIC MARKING DIAGRAM*



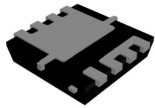
XXXX = Specific Device Code
A = Assembly Location
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

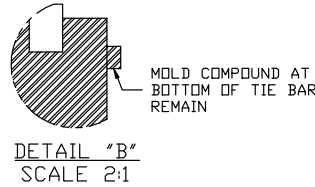
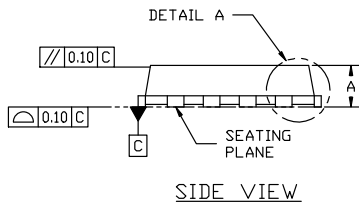
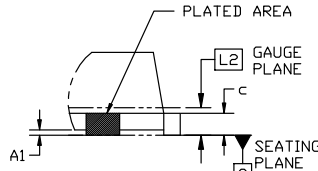
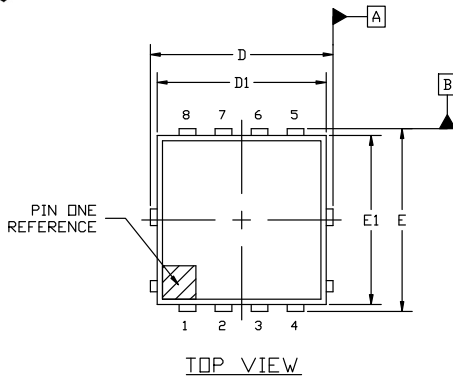


WDFNW8 3.30x3.30x0.75, 0.65P CASE 515AP ISSUE A

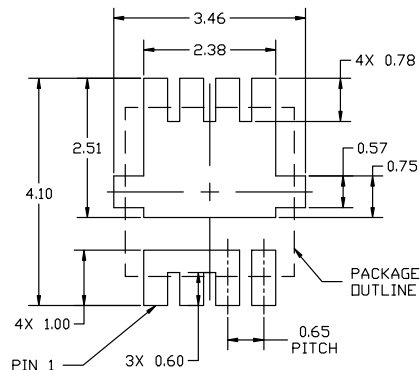
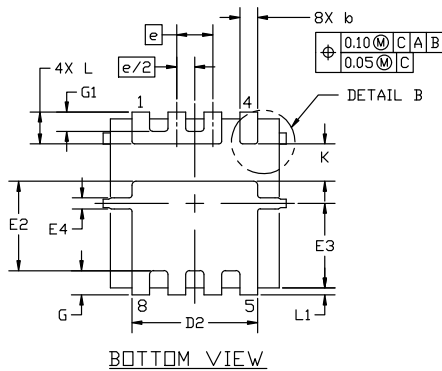
DATE 07 NOV 2023

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. FULL-CUT u8FL FUSED WF.



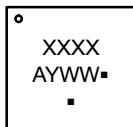
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E4	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
L2	0.25 BSC		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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