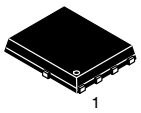
MOSFET – Power, Single N-Channel

60 V, 26 A, 24 mΩ

NVMFS5826NL

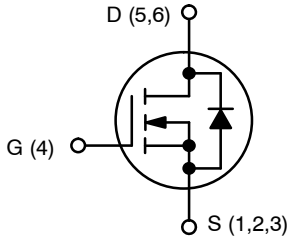
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	24 mΩ @ 10 V	26 A
	32 mΩ @ 4.5 V	



DFN5
(SO−8FL)
CASE 488AA
STYLE 1

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5826NLWF − Wettable Flanks Product
- AEC−Q101 Qualified and PPAP Capable
- These are Pb−Free Devices and RoHS Compliant



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain−to−Source Voltage			60	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State	T_{mb} = 25°C	26	A
			T_{mb} = 100°C	19	
P_D	Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)		T_{mb} = 25°C	39	W
			T_{mb} = 100°C	19	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	T_A = 25°C	8.0	A
			T_A = 100°C	6.0	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)		T_A = 25°C	3.6	W
			T_A = 100°C	1.8	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		130	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to + 175	°C
I_S	Source Current (Body Diode)			32	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 24 V, V_{GS} = 10 V, $I_{L(pk)}$ = 20 A, L = 0.1 mH, R_G = 25 Ω)			20	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

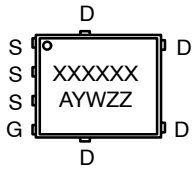
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\Psi J-mb}$	Junction−to−Mounting Board (top) − Steady State (Notes 2, 3)	3.9	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State (Note 3)	42	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = ± 20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.5		2.5	V
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 10 A			18	24	mΩ
		V_{GS} = 4.5 V, I_D = 10 A			24	32	
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 5 A			8.0		S
CHARGES AND CAPACITANCES							
C_{iss}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			850		pF
C_{oss}	Output Capacitance				85		
C_{rss}	Reverse Transfer Capacitance				50		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 10 A			9.1		nC
$Q_{G(TH)}$	Threshold Gate Charge				1.0		
Q_{GS}	Gate−to−Source Charge				3.0		
Q_{GD}	Gate−to−Drain Charge				4.0		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 10 A			17		nC
SWITCHING CHARACTERISTICS (Note 6)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 10 A, R_G = 2.5 Ω			9.0		ns
t_r	Rise Time				32		
$t_{d(OFF)}$	Turn−Off Delay Time				15		
t_f	Fall Time				24		
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 10 A			15		ns
t_a	Charge Time				11		
t_b	Discharge Time				4.0		
Q_{RR}	Reverse Recovery Charge				11		nC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

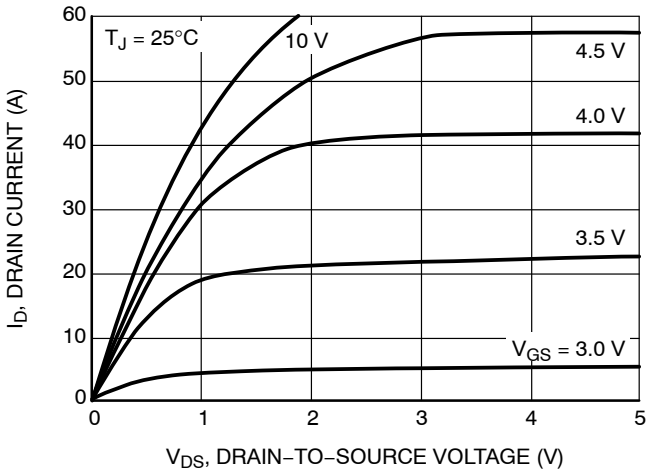


Figure 1. On−Region Characteristics

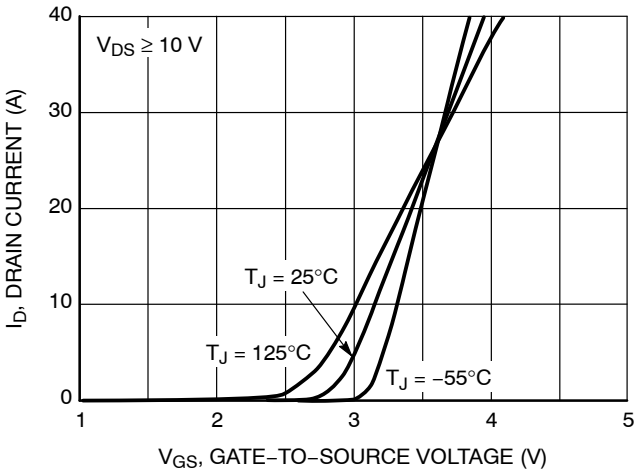


Figure 2. Transfer Characteristics

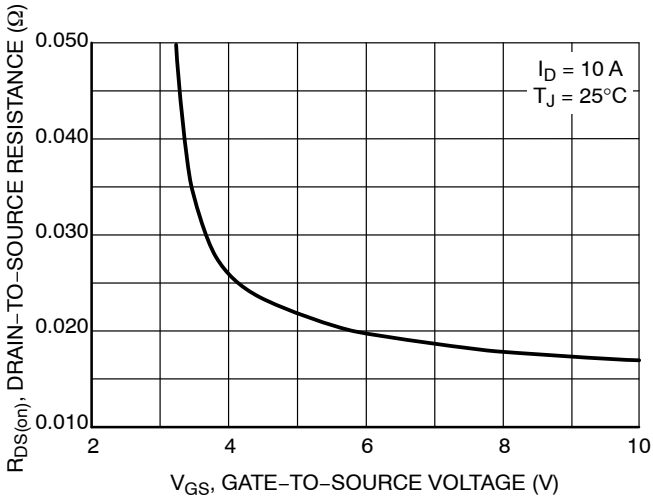


Figure 3. On−Resistance vs. Gate−to−Source Voltage

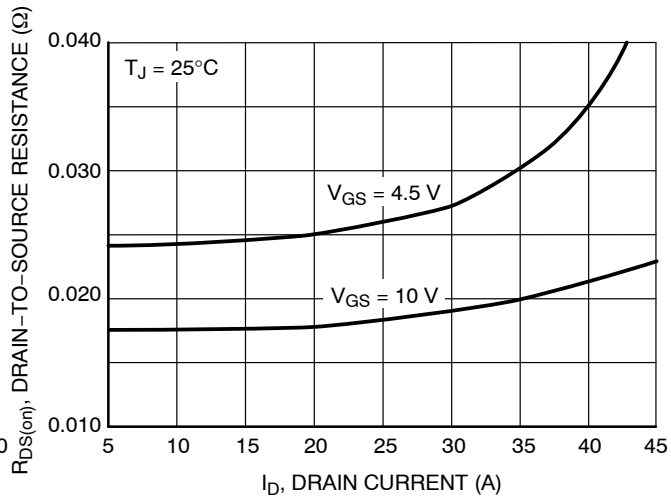


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

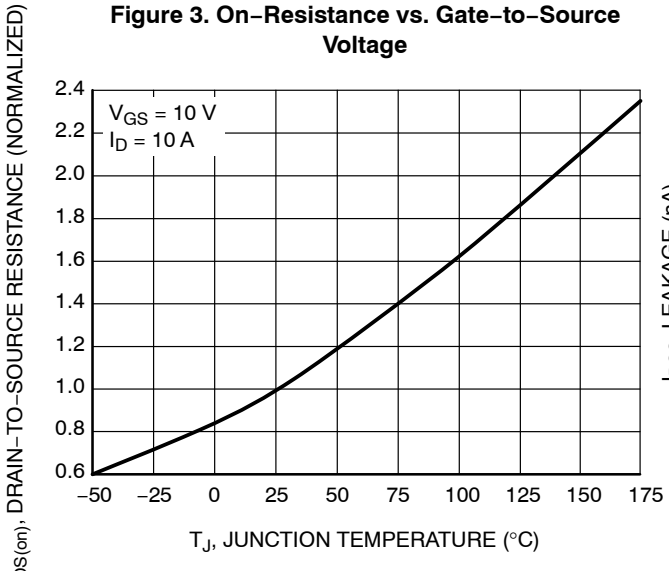


Figure 5. On−Resistance Variation with Temperature

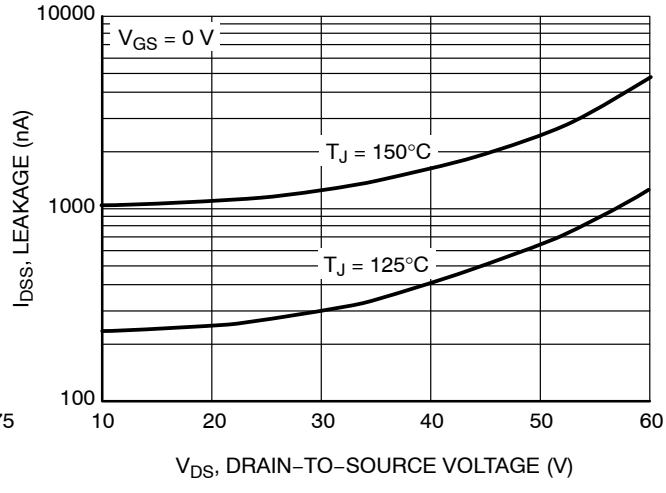


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

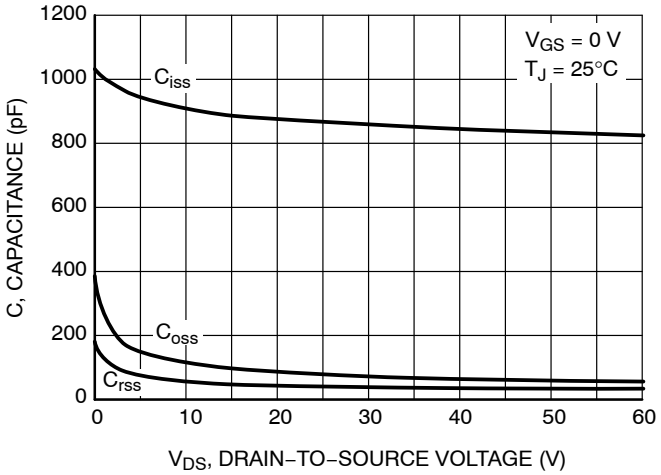


Figure 7. Capacitance Variation

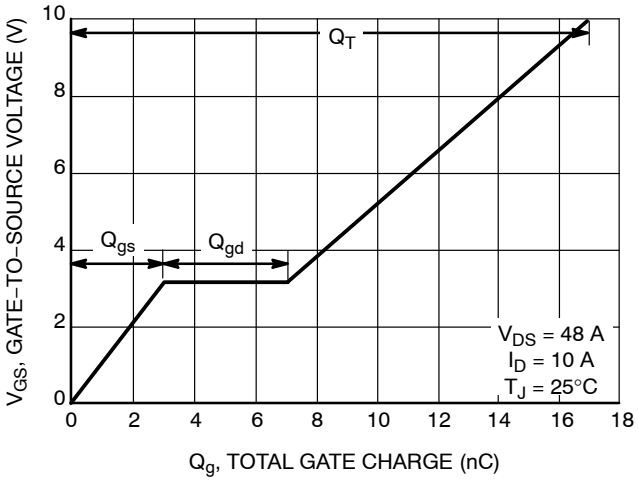


Figure 8. Gate−to−Source Voltage vs. Total Charge

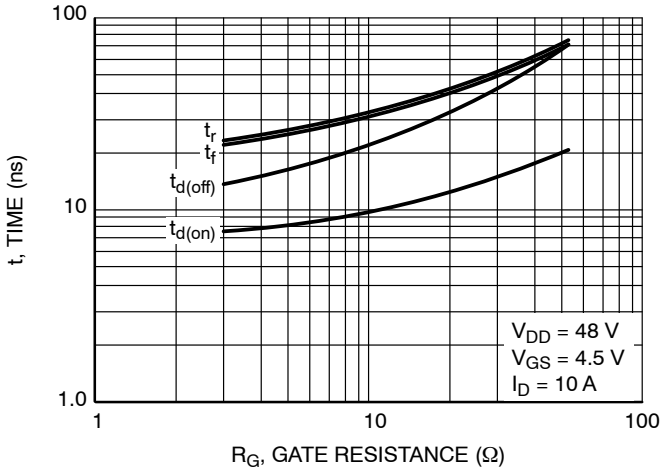


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

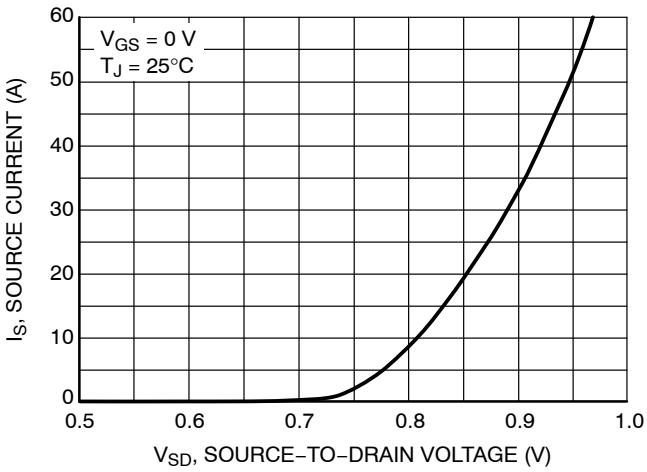


Figure 10. Diode Forward Voltage vs. Current

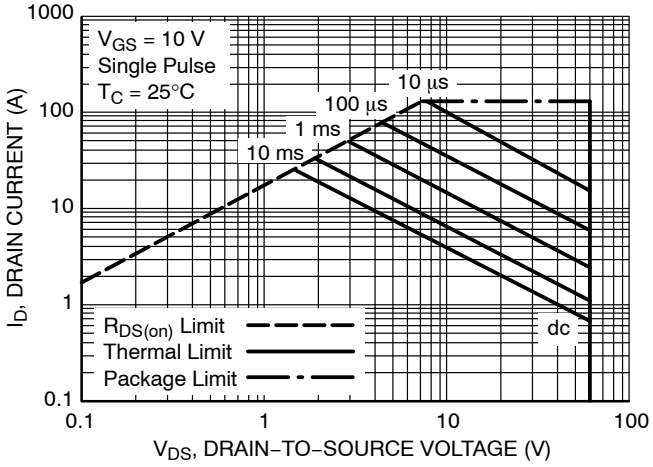


Figure 11. Maximum Rated Forward Biased Safe Operating Area

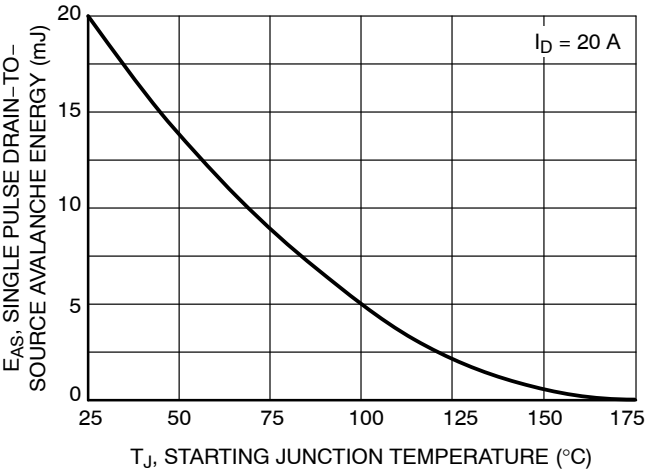


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS (continued)

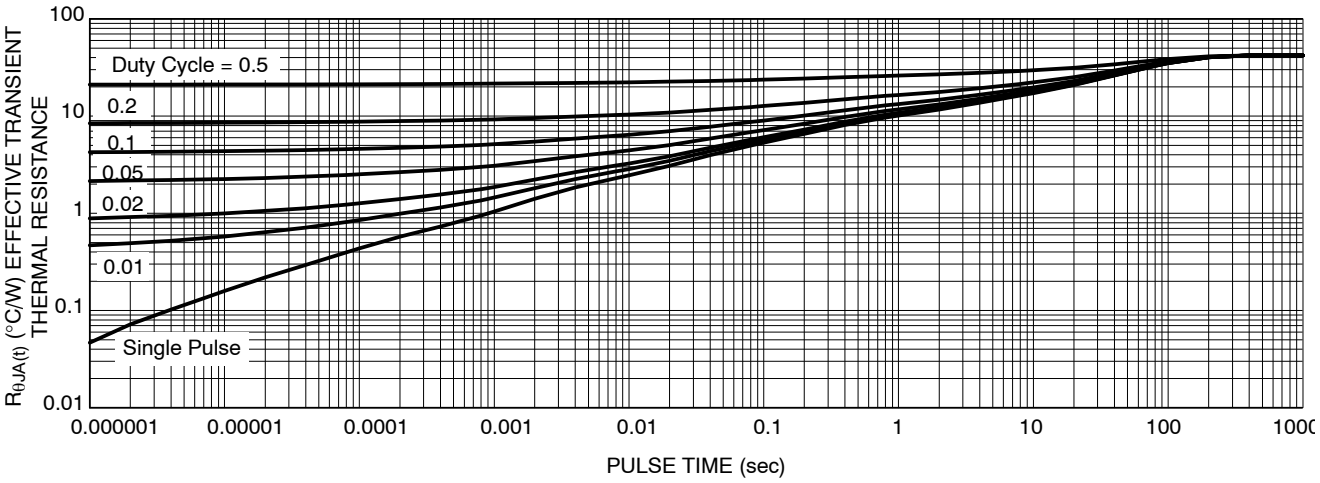


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

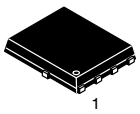
Device	Marking	Package	Shipping†
NVMFS5826NLWFT1G	5826LW	DFN5 (Pb−Free)	1500 / Tape & Reel

DISCONTINUED (Note 7)

NVMFS5826NLT1G	V5826L	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5826NLT3G	V5826L	DFN5 (Pb−Free)	5000 / Tape & Reel
NVMFS5826NLWFT3G	5826LW	DFN5 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

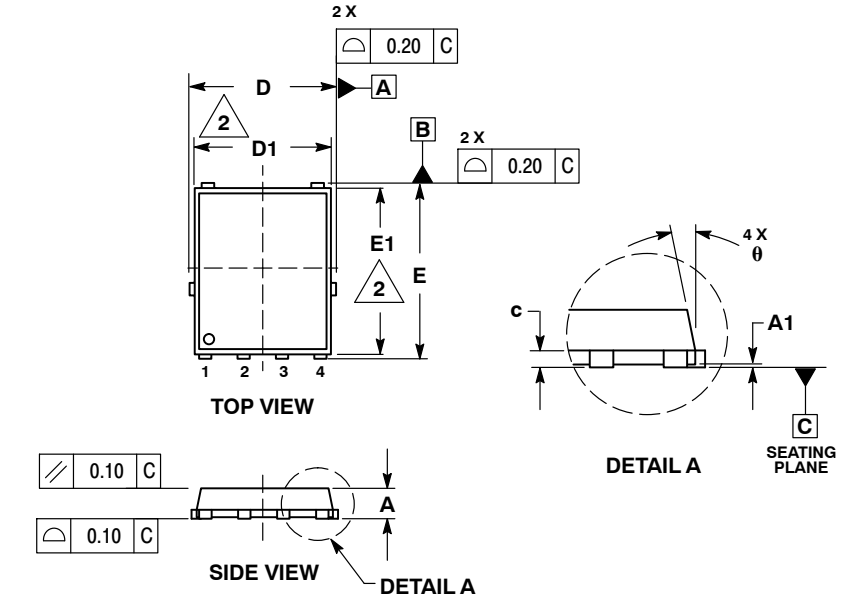
7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



SCALE 2:1

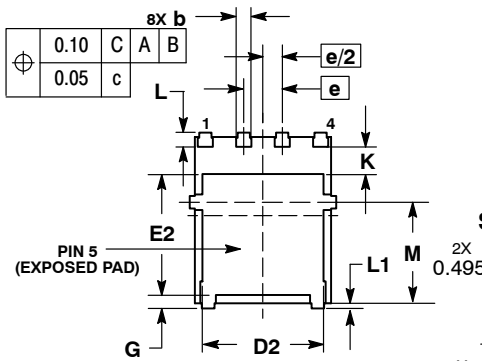
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

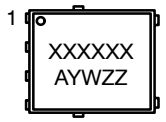


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °



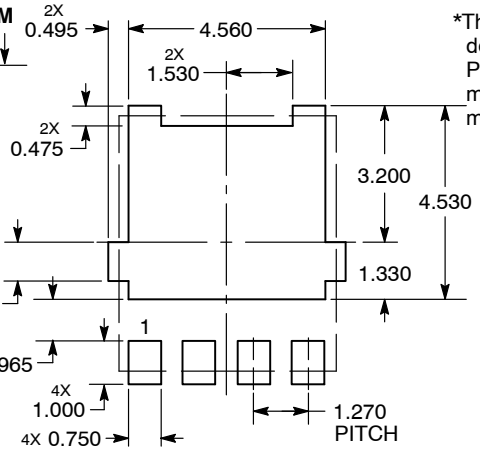
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON14036D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales