

# NVD5484NL

## Power MOSFET

60 V, 17 mΩ, 54 A, Single N-Channel  
Logic Level, DPAK

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	60	V
Gate-to-Source Voltage			V <sub>GS</sub>	± 20	V
Continuous Drain Current R <sub>θJC</sub> (Notes 1 & 3)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	54	A
		T <sub>C</sub> = 100°C		38	
Power Dissipation R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 25°C	P <sub>D</sub>	100	W
		T <sub>C</sub> = 100°C		50	
Continuous Drain Current R <sub>θJA</sub> (Notes 1, 2 & 3)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	10.7	A
		T <sub>A</sub> = 100°C		7.6	
Power Dissipation R <sub>θJA</sub> (Notes 1 & 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	3.9	W
		T <sub>A</sub> = 100°C		2.0	
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	305	A
Current Limited by Package (Note 3)	T <sub>A</sub> = 25°C		I <sub>Dmaxpkg</sub>	60	A
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	83	A
Single Pulse Drain-to-Source Avalanche Energy (T <sub>J</sub> = 25°C, V <sub>DD</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>L(pk)</sub> = 50 A, L = 0.1 mH, R <sub>G</sub> = 25 Ω)			E <sub>AS</sub>	125	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain)	$R_{\theta JC}$	1.5	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	38	

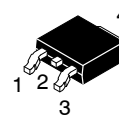
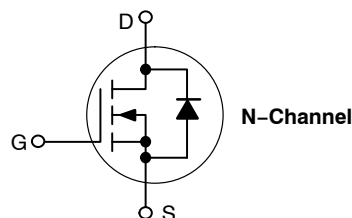
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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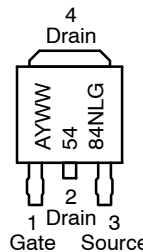
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$
60 V	17 mΩ @ 10 V	54 A
	23 mΩ @ 4.5 V	



DPAK  
CASE 369AA  
STYLE 2

### MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location\*  
Y = Year  
WW = Work Week  
5484NL = Device Code  
G = Pb-Free Package

\* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejector pin), the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NVD5484NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C		1.0 10	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.5	1.9	2.5	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 25 A		13.5 18	17 23	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		41		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		1410		pF
Output Capacitance	C <sub>oss</sub>			315		
Reverse Transfer Capacitance	C <sub>rss</sub>			135		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>DS</sub> = 48 V, I <sub>D</sub> = 23 A	V <sub>GS</sub> = 4.5 V V <sub>GS</sub> = 10 V	27 48		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 23 A		0.9		
Gate-to-Source Charge	Q <sub>GS</sub>			4.4		
Gate-to-Drain Charge	Q <sub>GD</sub>			19		
Gate Resistance	R <sub>G</sub>			8.5		Ω

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 23 A, R <sub>G</sub> = 10 Ω		18		ns
Rise Time	t <sub>r</sub>			160		
Turn-Off Delay Time	t <sub>d(off)</sub>			100		
Fall Time	t <sub>f</sub>			110		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 23 A, R <sub>G</sub> = 10 Ω		7.8		
Rise Time	t <sub>r</sub>			45		
Turn-Off Delay Time	t <sub>d(off)</sub>			152		
Fall Time	t <sub>f</sub>			113		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 25 A	T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C	0.9 0.8	1.2	V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 23 A		64		ns
Charge Time	t <sub>a</sub>			33		
Discharge Time	t <sub>b</sub>			31		
Reverse Recovery Charge	Q <sub>RR</sub>			118		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

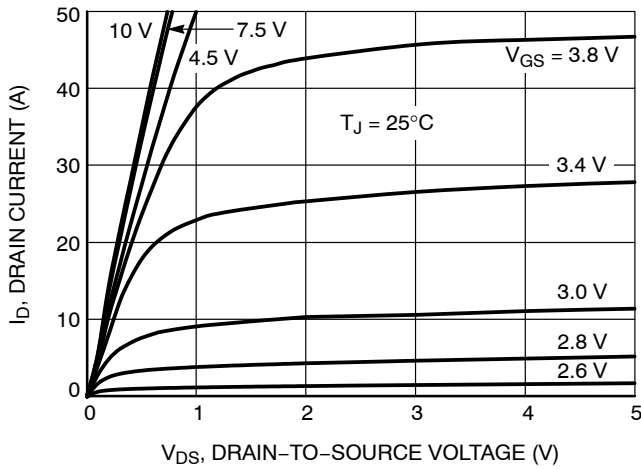


Figure 1. On-Region Characteristics

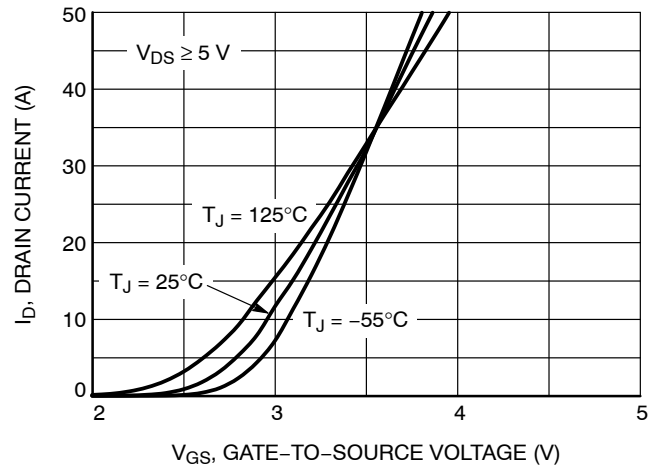


Figure 2. Transfer Characteristics

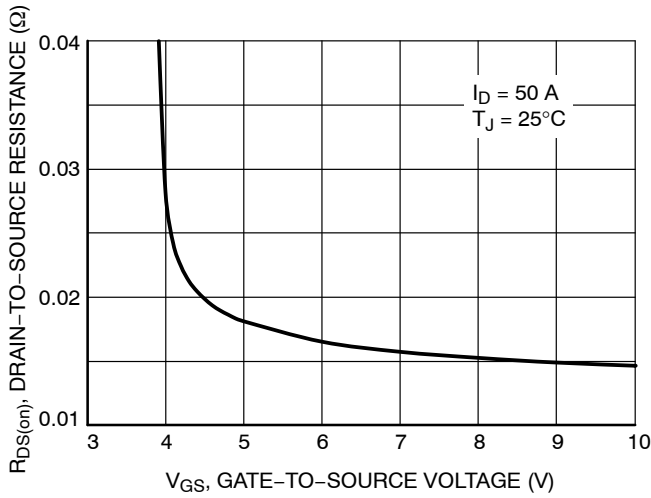


Figure 3. On-Resistance vs. Gate-to-Source Voltage

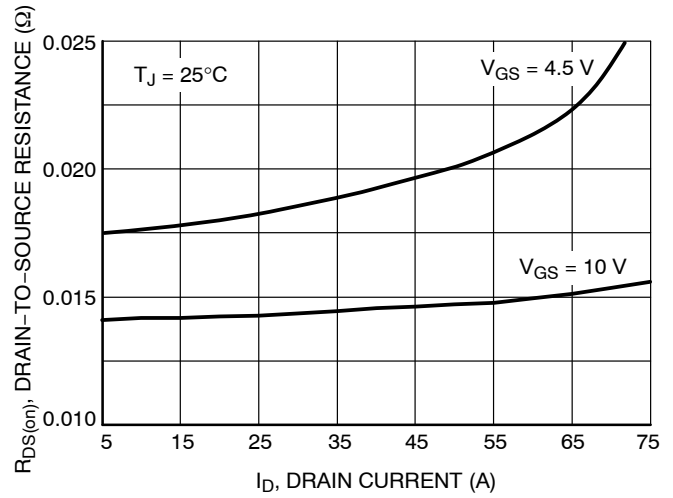


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

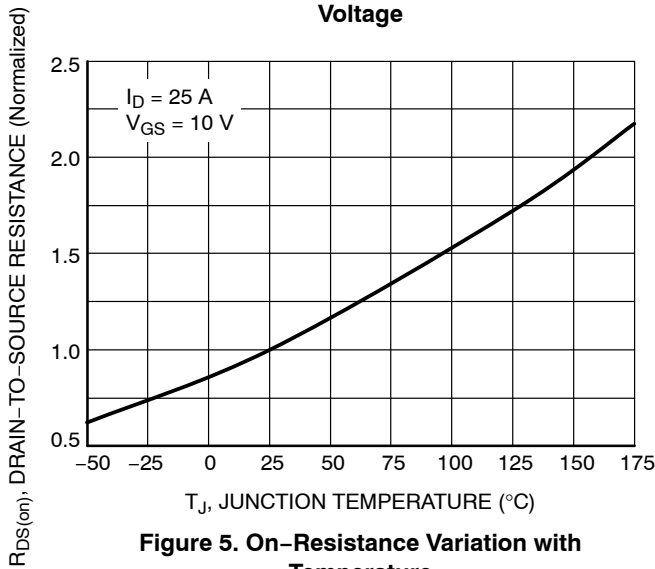


Figure 5. On-Resistance Variation with Temperature

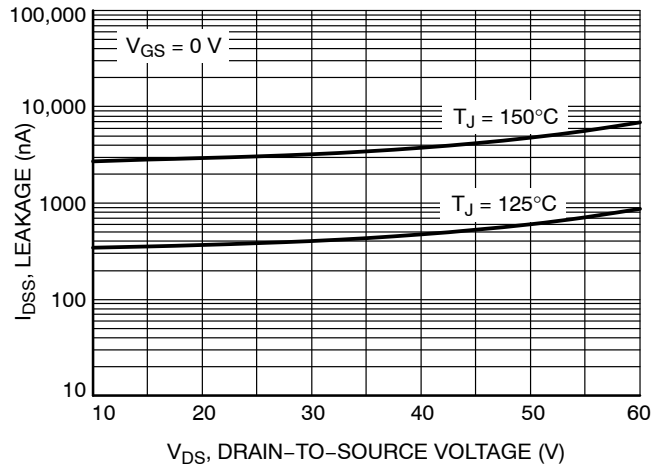


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

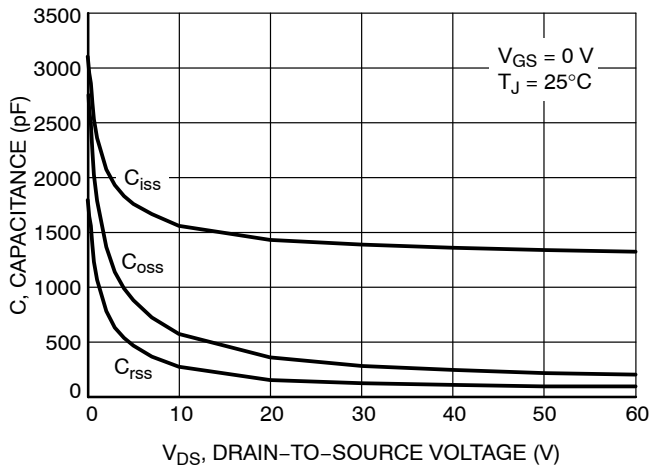


Figure 7. Capacitance Variation

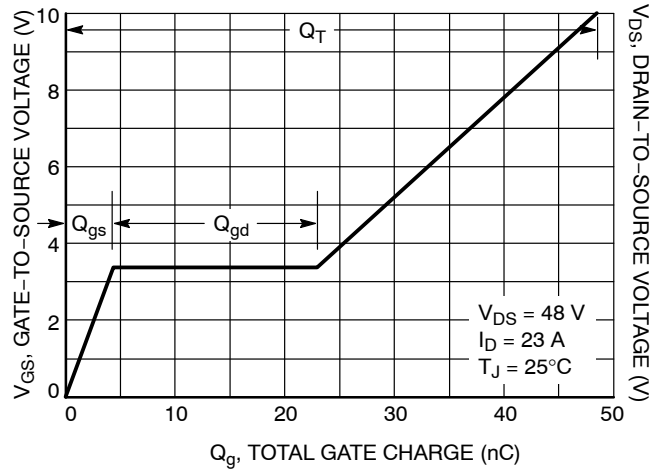


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

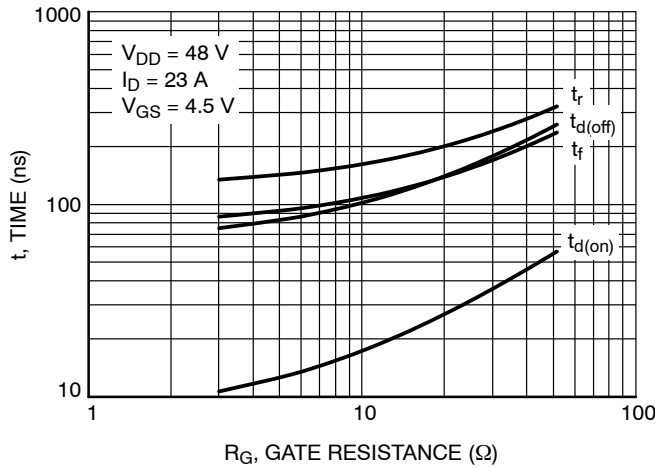


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

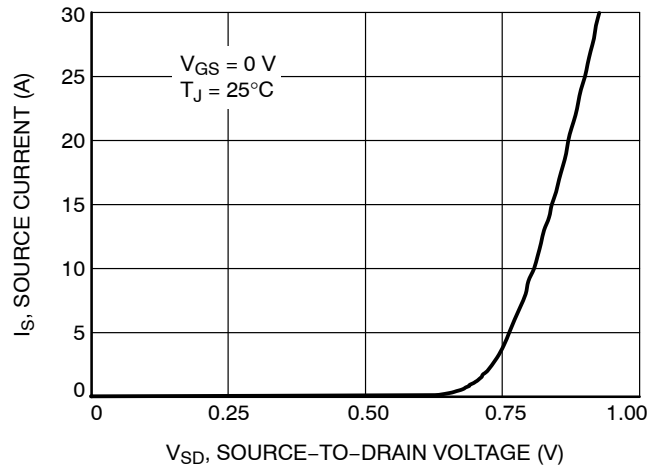


Figure 10. Diode Forward Voltage vs. Current

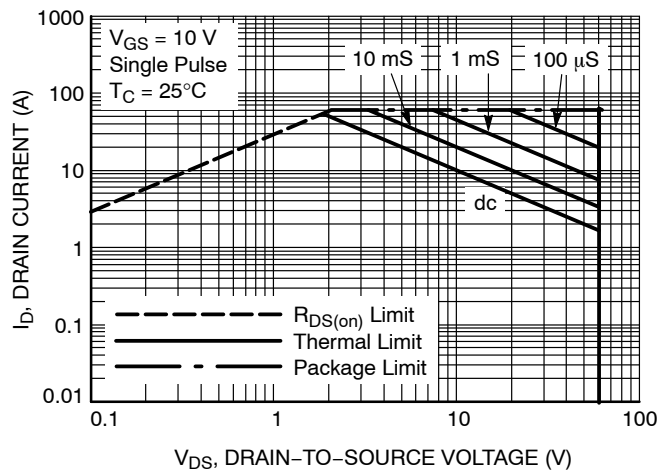
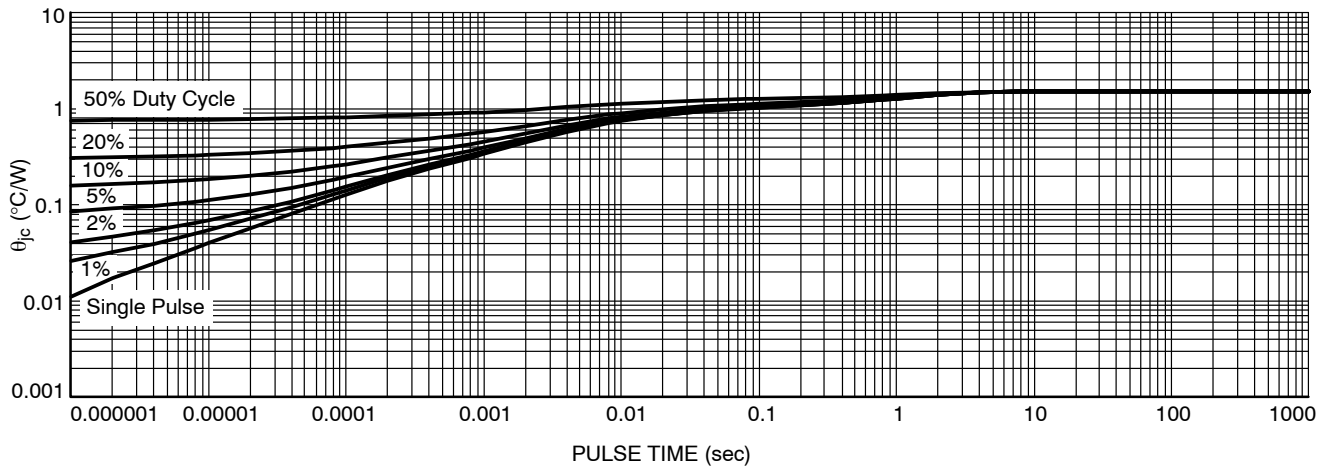


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NVD5484NL

## TYPICAL CHARACTERISTICS



**Figure 12. Thermal Response**

### ORDERING INFORMATION

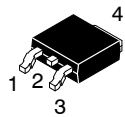
Order Number	Package	Shipping <sup>†</sup>
NVD5484NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5484NLT4G-VF01	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

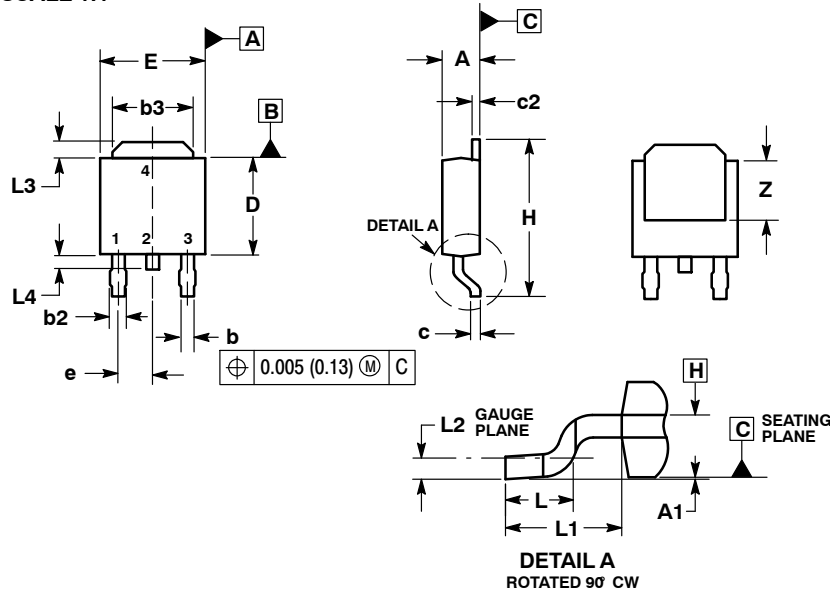
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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ON



SCALE 1:1



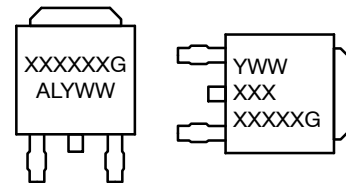
## NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	0.040	0.040	1.01	1.01
Z	0.155		3.93	

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

## GENERIC MARKING DIAGRAM\*



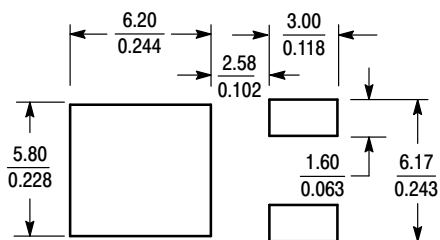
IC

Discrete

- XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

## SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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