

MOSFET – Power, N-Channel, SUPERFET® III, Easy Drive

650 V, 260 mΩ, 12 A

NVD260N65S3

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on) max.} \times Q_{g typ.}$ & $R_{DS(on) max.} \times E_{OSS}$)
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	650	V
Gate-to-Source Voltage – DC	V_{GSS}	± 30	V
Gate-to-Source Voltage – AC ($f > 1$ Hz)	V_{GSS}	± 30	V
Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	I_D	12	A
Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	I_D	7.6	A
Drain Current – Pulsed (Note 3)	I_{DM}	30	A
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	90	W
Power Dissipation – Derate Above 25°C	P_D	0.72	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	57	mJ
Repetitive Avalanche Energy (Note 3)	E_{AR}	0.9	mJ
MOSFET dv/dt	dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)	dv/dt	20	V/ns
Max. Lead Temperature for Soldering Purposes (1/8" from case for 5 s)	T_L	300	$^\circ\text{C}$

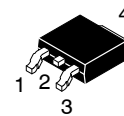
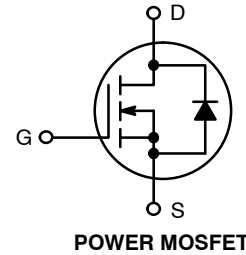
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max. (Notes 1, 2)	$R_{\theta JC}$	1.39	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, Max. (Notes 1, 2, 6)	$R_{\theta JA}$	40	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

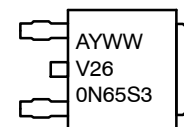
1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse-width limited by maximum junction temperature.
4. $I_{AS} = 2.3$ A, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
5. $I_{SD} \leq 6$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq 400$ V, starting $T_J = 25^\circ\text{C}$.
6. Device on 1 in² pad 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

V_{DSS}	$R_{DS(ON) MAX}$	$I_D MAX$
650 V	260 mΩ @ 10 V	12 A



DPAK
CASE 369C

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- V260N65S3 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NVD260N65S3T4G	DPAK3 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVD260N65S3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D = 1 mA, Referenced to 25°C		660		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 650 V			1	μA
		V _{DS} = 520 V, T _C = 125°C		0.77		
Gate-to-Body Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 0.29 mA	2.5		4.5	V
Threshold Temperature Coefficient	ΔV _{GS(th)} /ΔT _J	V _{GS} = V _{DS} , I _D = 0.29 mA		-8.9		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 6 A		217	260	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 20 V, I _D = 6 A		7.3		S

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 400 V, f = 1 MHz		1042		pF
Output Capacitance	C _{oss}			22.5		
Reverse Transfer Capacitance	C _{rss}			3.8		
Effective Output Capacitance	C _{oss(eff.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		225		pF
Energy Related Output Capacitance	C _{oss(er.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		37.5		pF
Total Gate Charge at 10 V	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 400 V, I _D = 6 A (Note 7)		23.5		nC
Threshold Gate Charge	Q _{G(TH)}			3.8		
Gate-to-Source Gate Charge	Q _{GS}			6.3		
Gate-to-Drain "Miller" Charge	Q _{GD}			9.8		
Equivalent Series Resistance	ESR	f = 1 MHz		8.1		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 400 V, I _D = 6 A, R _g = 4.7 Ω (Note 7)		17.2		ns
Turn-On Rise Time	t _r			13.9		ns
Turn-Off Delay Time	t _{d(off)}			48.3		ns
Turn-Off Fall Time	t _f			8.3		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

Maximum Continuous Source-to-Drain Diode Forward Current	I _S	V _{GS} = 0 V			12	A
Maximum Pulsed Source-to-Drain Diode Forward Current	I _{SM}	V _{GS} = 0 V			30	A
Source-to-Drain Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 6 A			1.2	V
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _F /dt = 100 A/μs, I _{SD} = 6 A		232		ns
Charge Time	t _a			220		
Discharge Time	t _b			13		
Reverse Recovery Charge	Q _{rr}			2837		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Essentially independent of operating temperature typical characteristics.

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TYPICAL CHARACTERISTICS

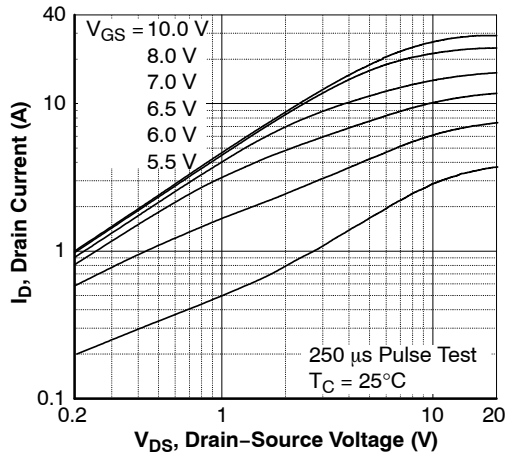


Figure 1. On-Region Characteristics 25°C

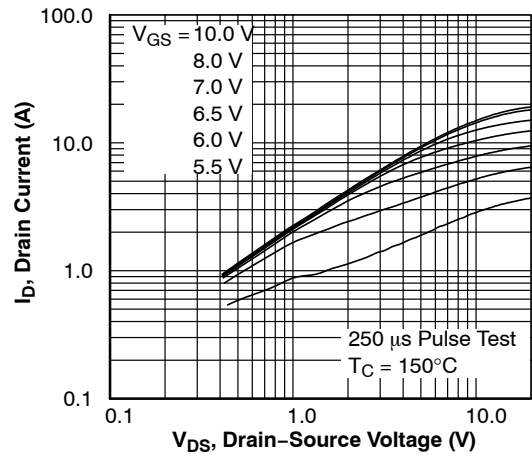


Figure 2. On-Region Characteristics 150°C

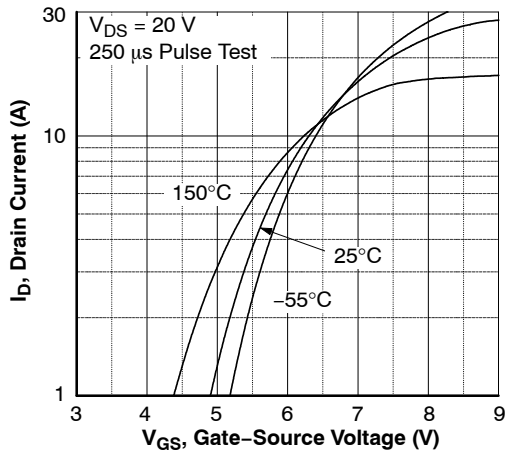


Figure 3. Transfer Characteristics

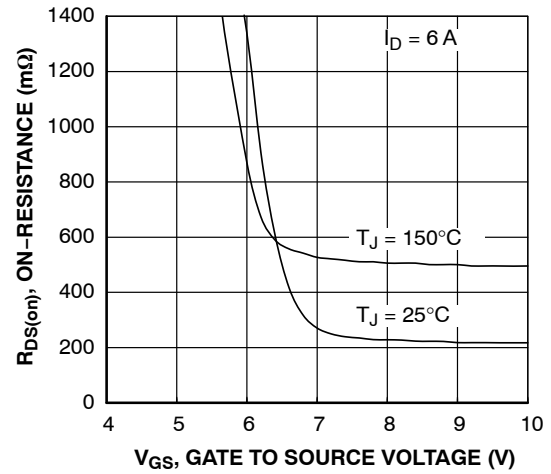


Figure 4. $R_{DS(on)}$ vs. Gate Voltage

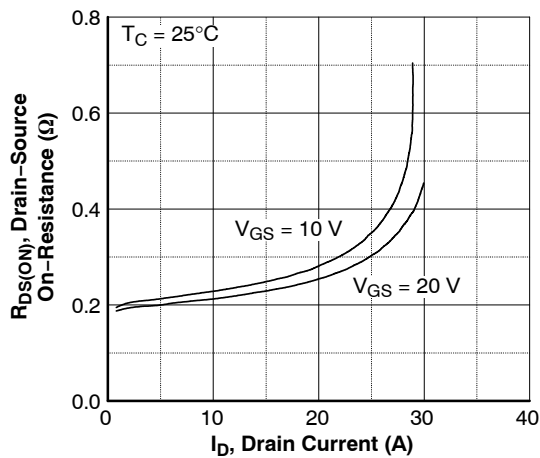


Figure 5. On-Resistance Variation vs. Drain Current and Gate Voltage

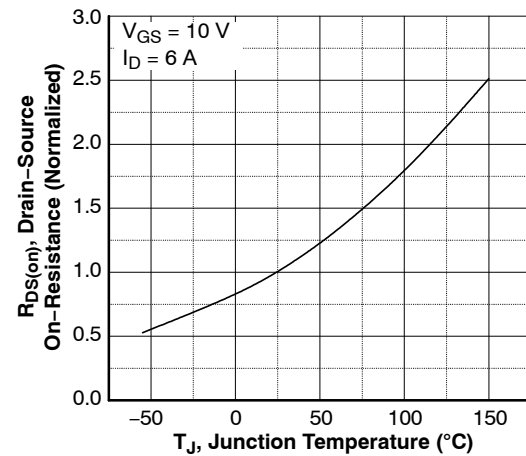


Figure 6. On-Resistance Variation vs. Temperature

TYPICAL CHARACTERISTICS

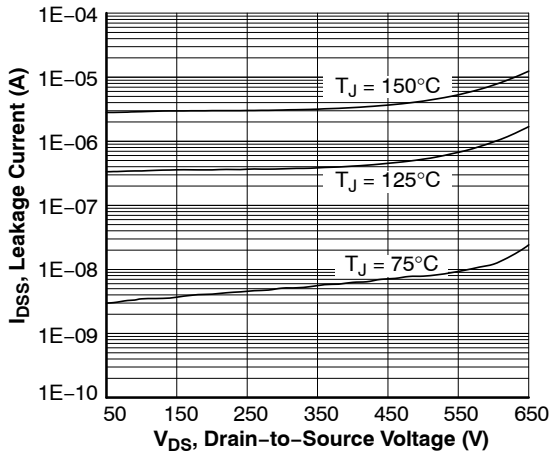


Figure 7. Drain-to-Source Leakage Current vs. Voltage

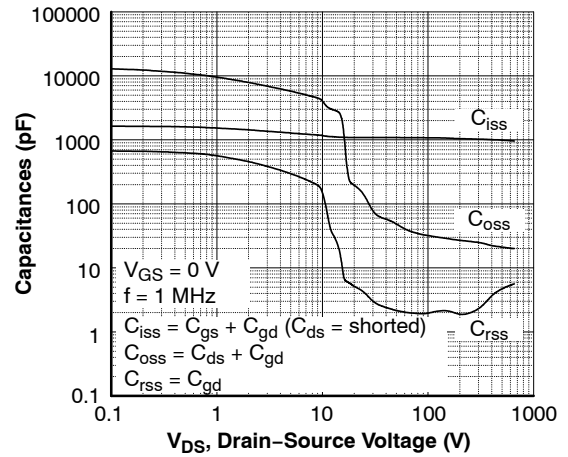


Figure 8. Capacitance Characteristics

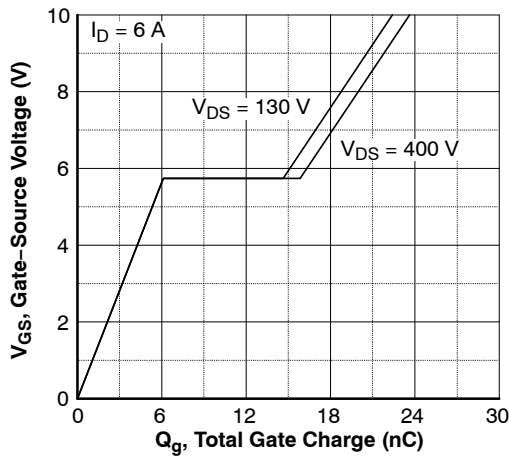


Figure 9. Gate Charge Characteristics

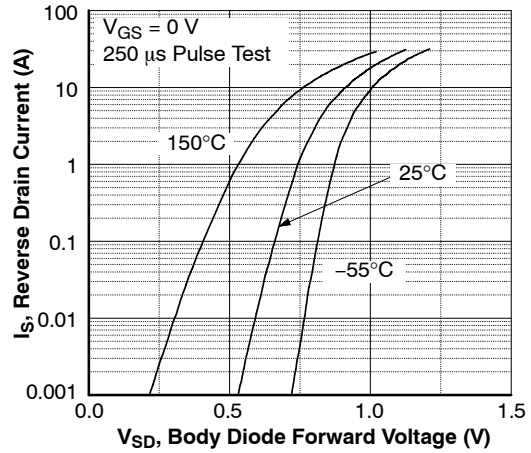


Figure 10. Body Diode Forward Voltage Variation vs. Source Current and Temperature

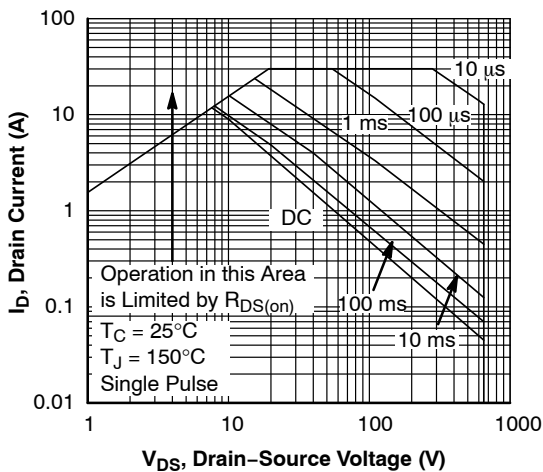


Figure 11. Maximum Safe Operating Area

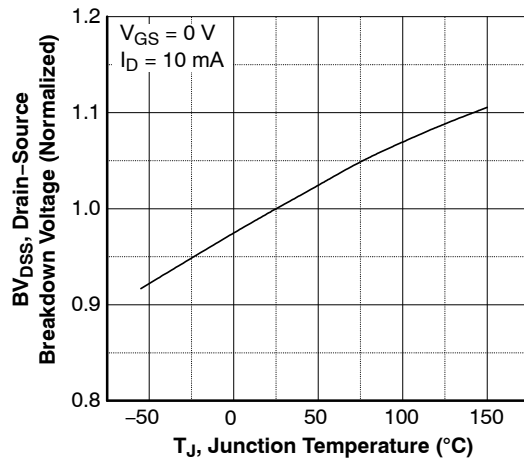


Figure 12. Breakdown Voltage Variation vs. Temperature

NVD260N65S3

TYPICAL CHARACTERISTICS

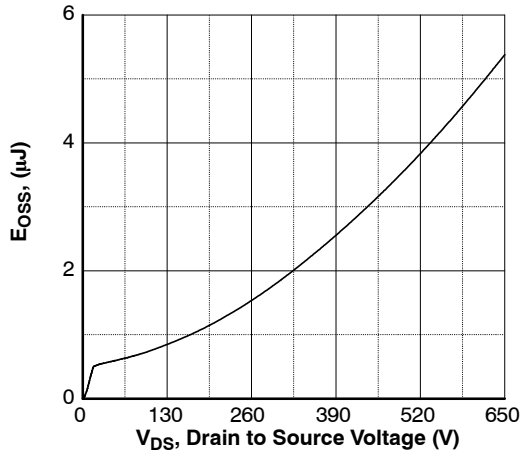


Figure 13. E_{OSS} vs. Drain to Source Voltage

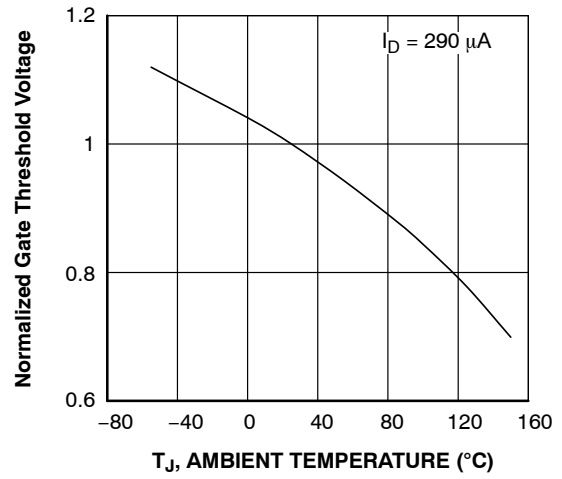


Figure 14. Normalized Gate Threshold Voltage vs. Temperature

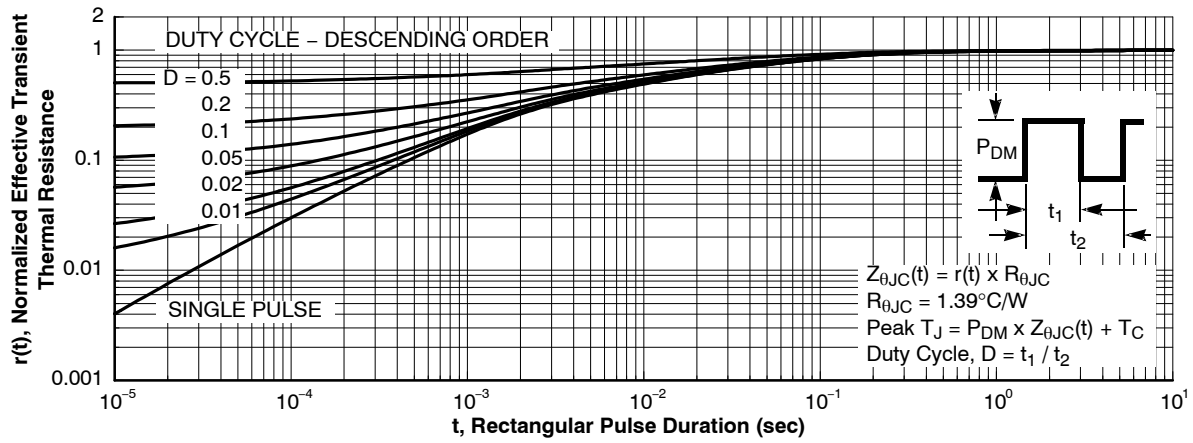


Figure 15. Transient Thermal Response Curve

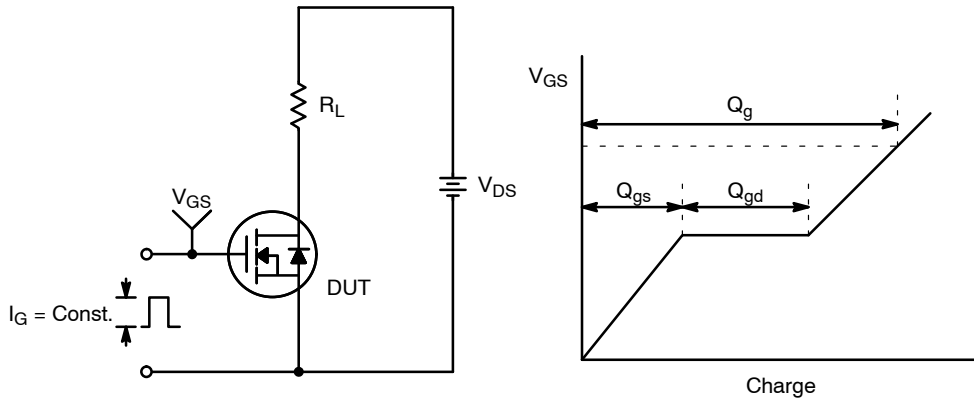


Figure 16. Gate Charge Test Circuit & Waveform

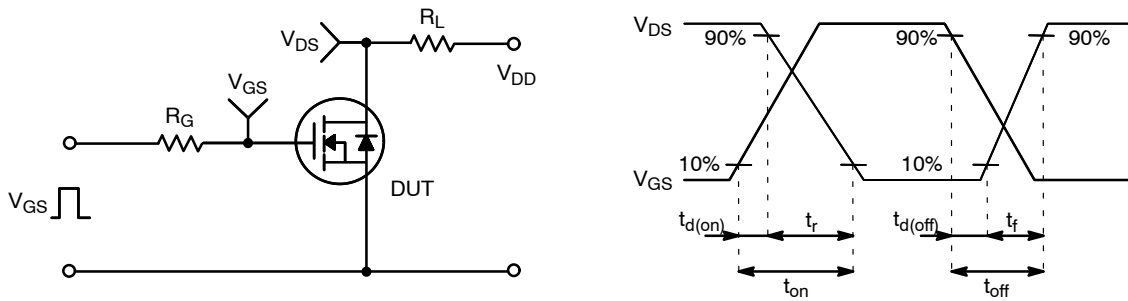


Figure 17. Resistive Switching Test Circuit & Waveforms

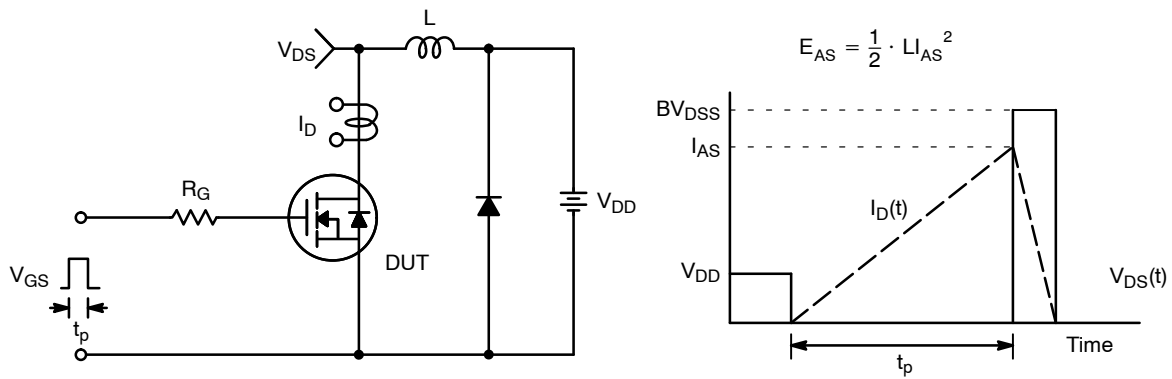


Figure 18. Unclamped Inductive Switching Test Circuit & Waveforms

NVD260N65S3

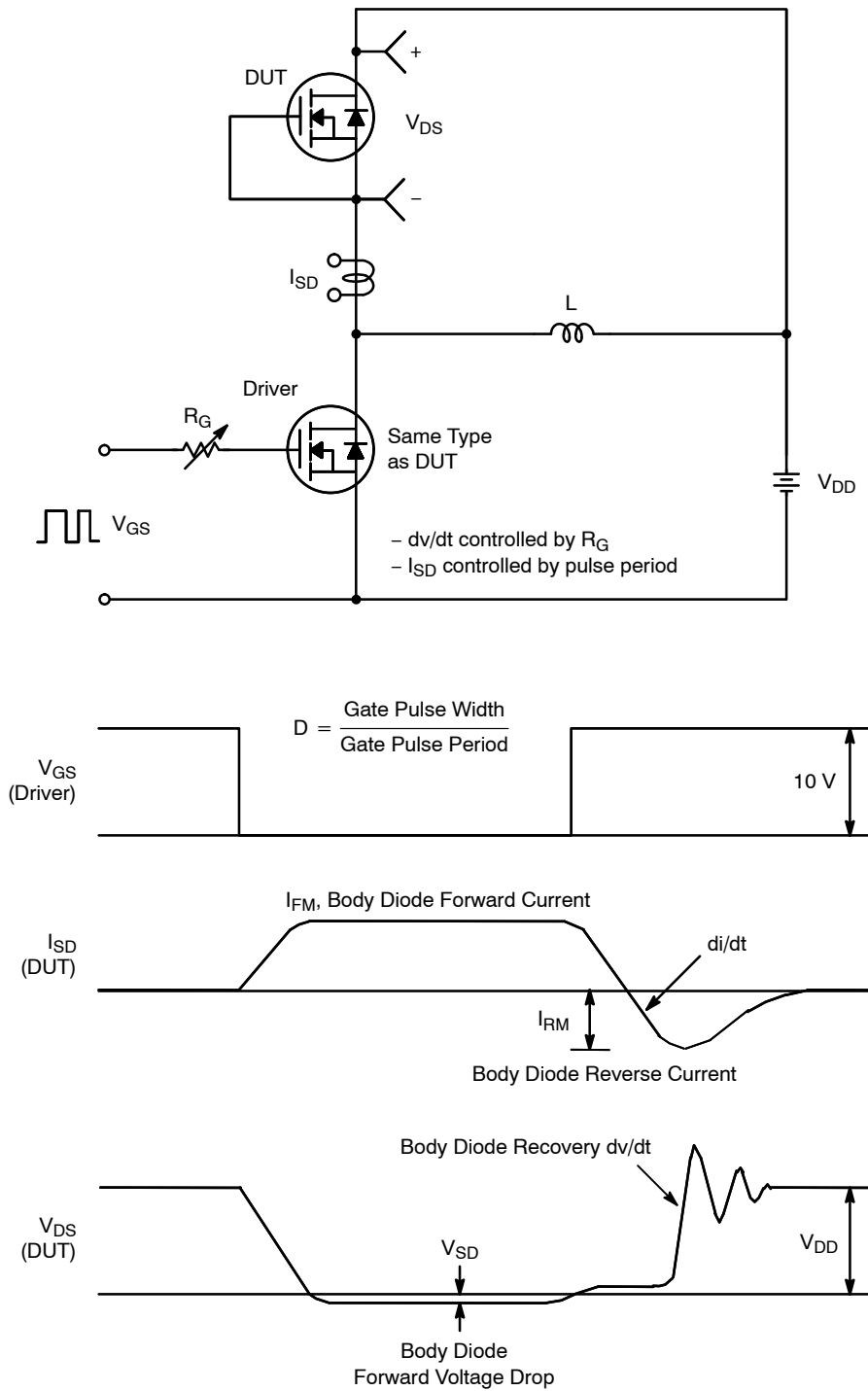
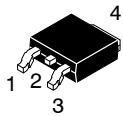


Figure 19. Peak Diode Recovery dv/dt Test Circuit & Waveforms

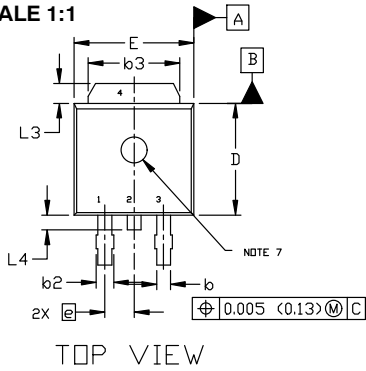
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



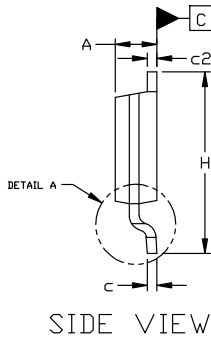
DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

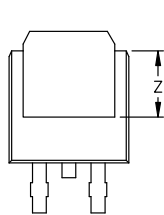
SCALE 1:1



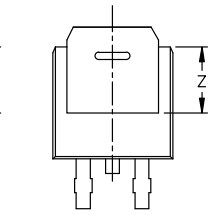
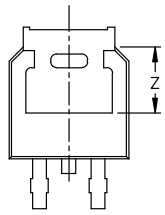
TOP VIEW



SIDE VIEW

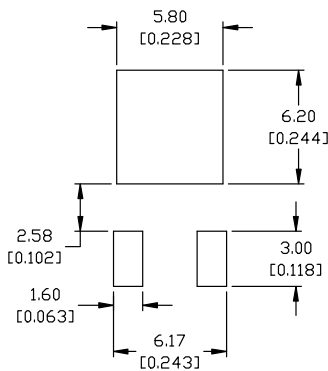


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 3:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 4:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 5:

- PIN 1. GATE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 6:

- PIN 1. MT1
- 2. MT2
- 3. GATE
- 4. MT2

STYLE 7:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 8:

- PIN 1. N/C
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 9:

- PIN 1. ANODE
- 2. CATHODE
- 3. RESISTOR ADJUST
- 4. CATHODE

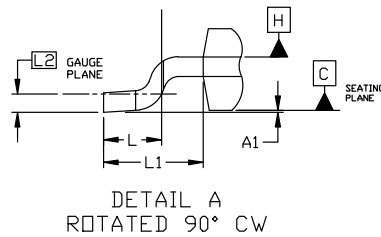
STYLE 10:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

NOTES:

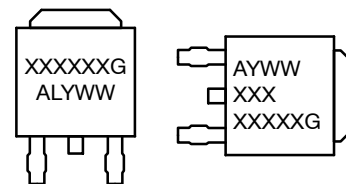
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



- IC
- Discrete
- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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