MOSFET - Power, Single N-Channel, TOLL

80 V, 0.79 mΩ, 457 A

NVBLS0D8N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	0.79 mΩ @ 10 V	457 A

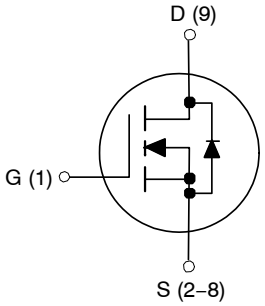
Features

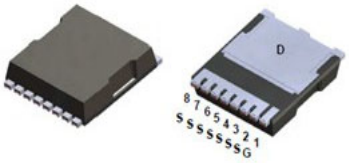
- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification (SR) in DC−DC and AC−DC
- Primary Switch in Isolated DC−DC Converter
- Motor Drives
- 48 V Battery Switch
- Battery Management System

N−CHANNEL MOSFET





H−PSOF8L
CASE 100CU

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	80	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	457	A
	T_C = 100°C		323	
Power Dissipation	T_C = 25°C	P_D	325	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	1629	A
Pulsed Source Current (Body Diode)		I_{SM}	1629	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)		I_S	547	A
Single Pulse Avalanche Energy (I_{PK} = 103 A)		E_{AS}	530	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. E_{AS} of 530 mJ is based on started T_J = 25°C, I_{AS} = 103 A, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

MARKING DIAGRAM

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
0D8N08 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NVBLS0D8N08XTXG	H−PSOF8L (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.46	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	43	

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		35.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25°C			2	μA
		V_{DS} = 80 V, T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 80 A, T_J = 25°C		0.69	0.79	mΩ
Gate Threshold Voltage		V_{GS} = V_{DS}, I_D = 720 μA, T_J = 25°C	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 720 μA		−7.95		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 80 A		485		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{iss}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		12920		pF
Output Capacitance	C_{oss}			3670		
Reverse Transfer Capacitance	C_{rss}			55		
Output Charge	Q_{oss}			262		nC
Total Gate Charge	$Q_{G(tot)}$	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 6 V		109		
		V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V		174		
Threshold Gate Charge	$Q_{G(th)}$			34		
Gate−to−Source Charge	Q_{gs}			54		
Gate−to−Drain Charge	Q_{gd}			32		
Gate Plateau Voltage	V_{gp}			4.6		V
Gate Resistance	R_g	f = 1 MHz		0.5		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(on)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 80 A, R_G = 2.5 Ω		35		ns
Rise Time	t_r			15		
Turn−Off Delay Time	$t_{d(off)}$			74		
Fall Time	t_f			20		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_S = 80 A, V_{GS} = 0 V, T_J = 25°C		0.8		V
		I_S = 80 A, V_{GS} = 0 V, T_J = 125°C		0.66		
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, I_S = 80 A dI/dt = 1000 A/μs, V_{DD} = 64 V		57		ns
Charge Time	t_a			26		
Discharge Time	t_b			31		
Reverse Recovery Charge	Q_{rr}			650		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

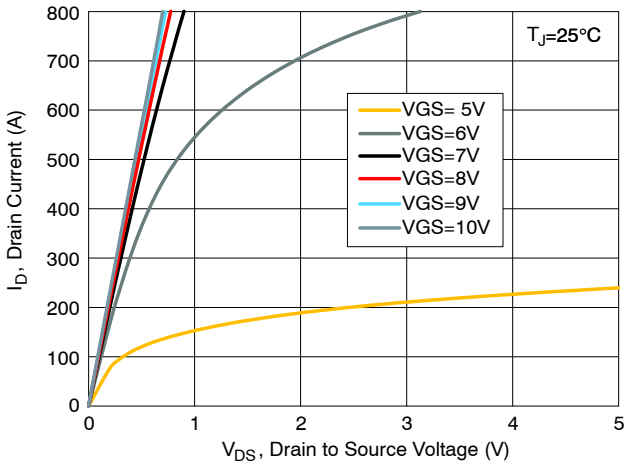


Figure 1. On−Region Characteristics

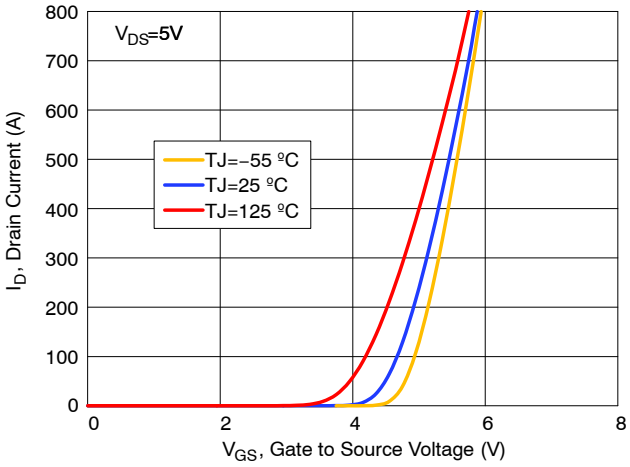


Figure 2. Transfer Characteristics

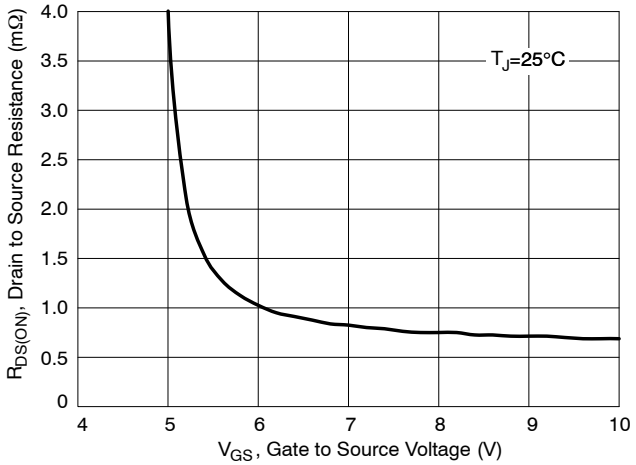


Figure 3. On−Resistance vs. Gate Voltage

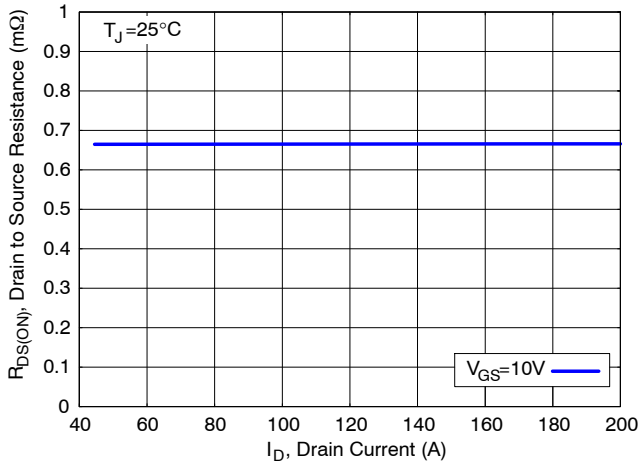


Figure 4. On−Resistance vs. Drain Current

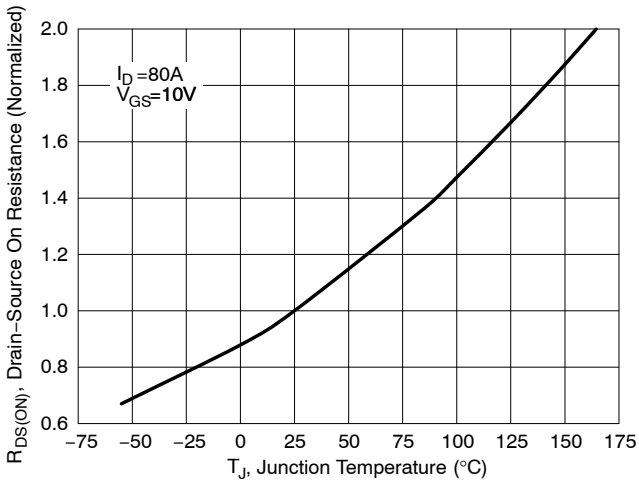


Figure 5. Normalized On−Resistance vs. Junction Temperature

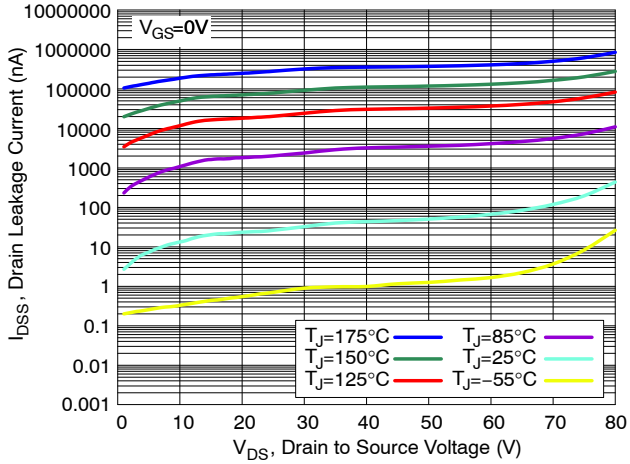


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

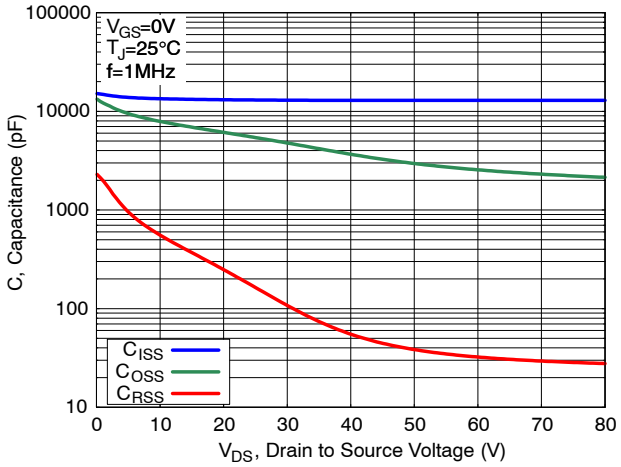


Figure 7. Capacitance Characteristics

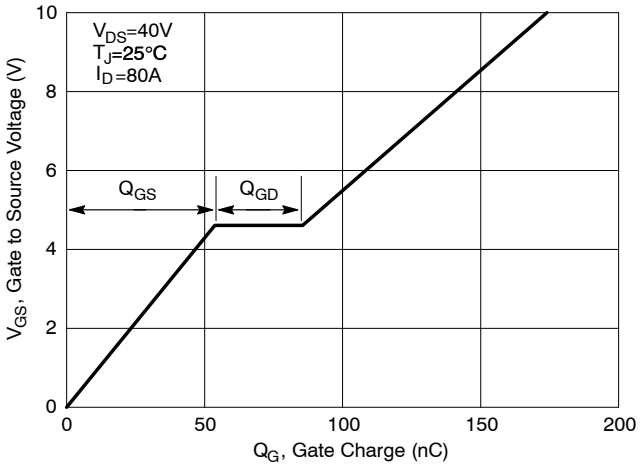


Figure 8. Gate Charge Characteristics

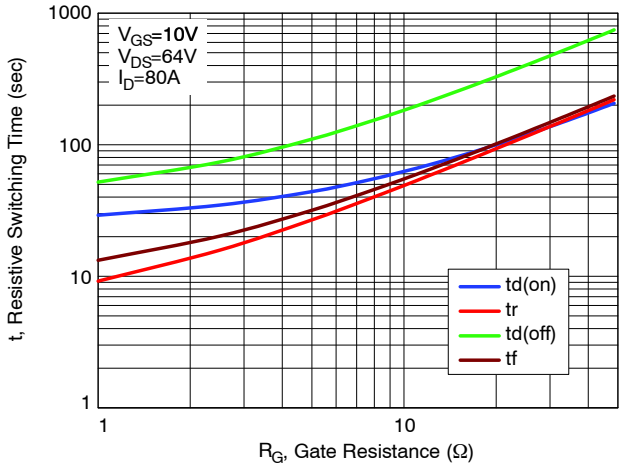


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

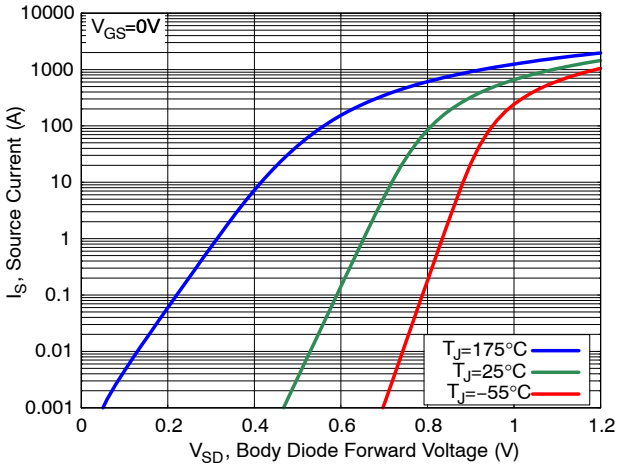


Figure 10. Diode Forward Characteristics

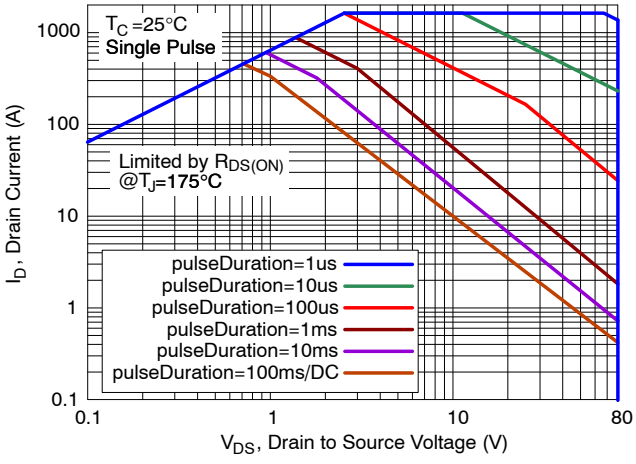


Figure 11. Safe Operating Area (SOA)

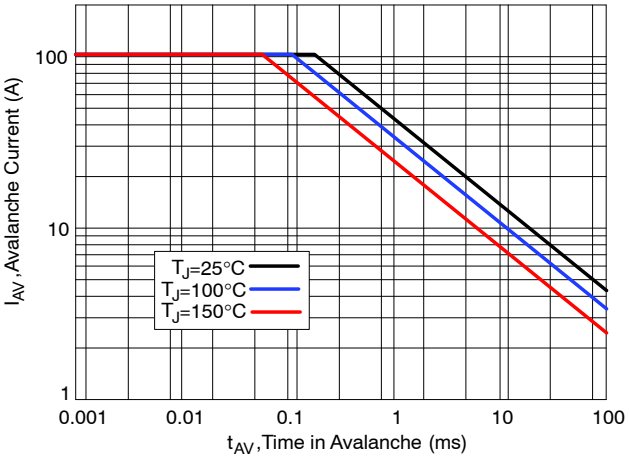


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

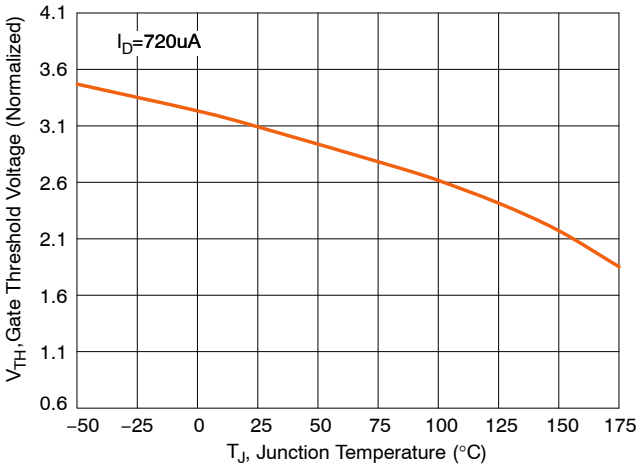


Figure 13. Gate Threshold Voltage vs. Junction Temperature

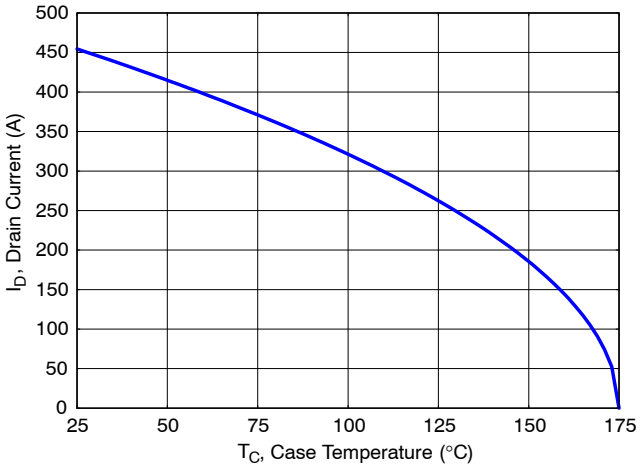


Figure 14. Maximum Current vs. Case Temperature

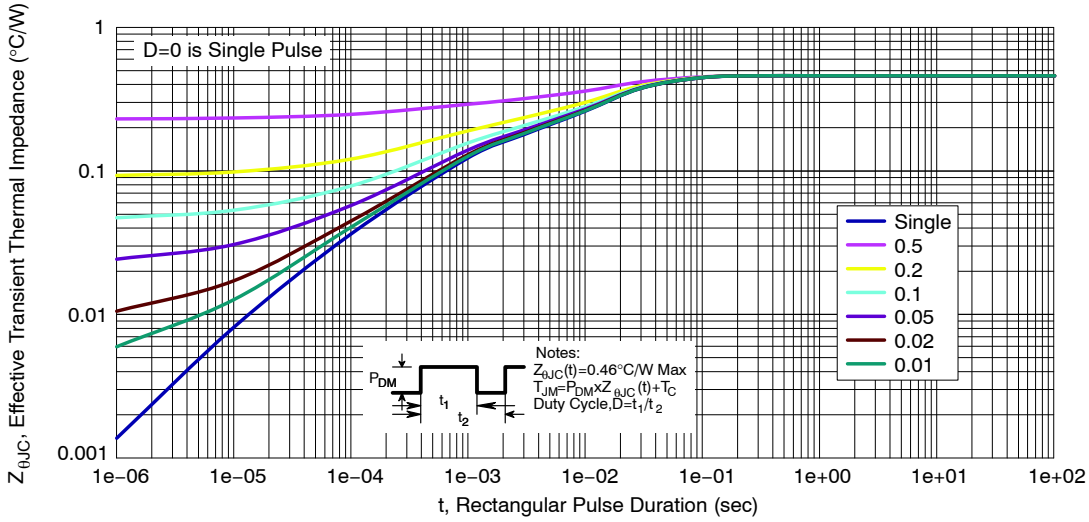
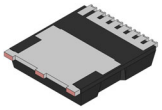
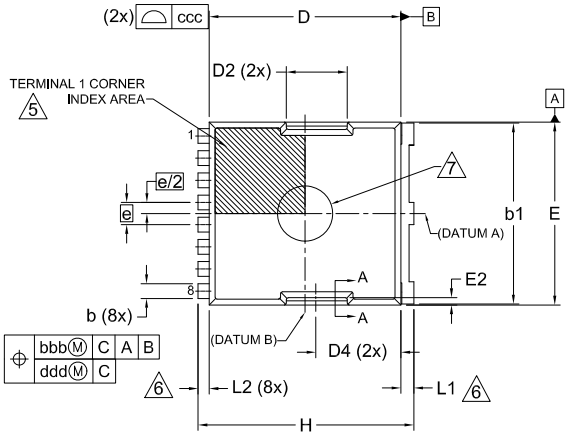


Figure 15. Transient Thermal Response

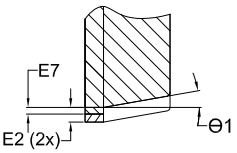


H−PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

DATE 30 JUL 2024



TOP VIEW



SECTION "A-A"
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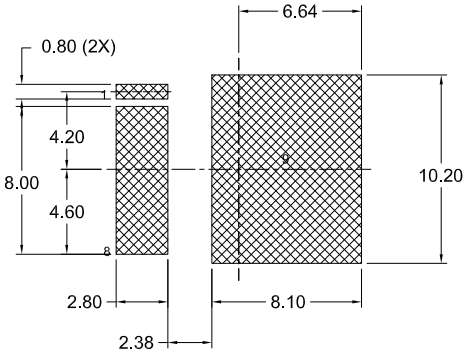
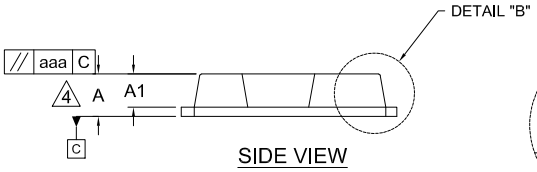
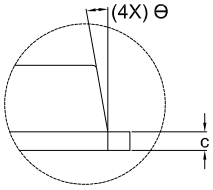


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



SIDE VIEW



DETAIL "B"
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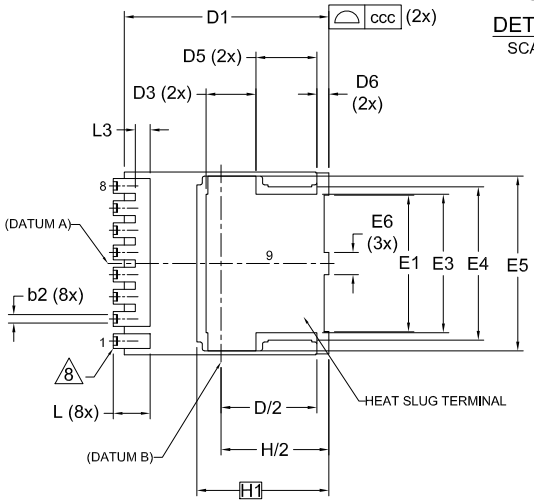


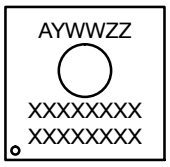
BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g.,EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13813G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**H−PSOF8L 11.68x9.80x2.30, 1.20P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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