

# NUS5530MN

## Integrated Power MOSFET with PNP Low $V_{CE(sat)}$ Switching Transistor

This integrated device represents a new level of safety and board-space reduction by combining the 20 V P-Channel FET with a PNP Silicon Low  $V_{CE(sat)}$  switching transistor. This newly integrated product provides higher efficiency and accuracy for battery powered portable electronics.

### Features

- Low  $R_{DS(on)}$  (MOSFET) and Low  $V_{CE(sat)}$  (Transistor)
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive (MOSFET)
- Performance DFN Package
- This is a Pb-Free Device

### Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS FOR P-CHANNEL FET

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	5 sec	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-20		V
Gate-Source Voltage	$V_{GS}$	$\pm 12$		V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$I_D$	-5.3 -3.8	-3.9 -2.8	A
Pulsed Drain Current	$I_{DM}$	$\pm 20$		A
Continuous Source Current (Note 1)	$I_S$	-5.3	-3.9	A
Maximum Power Dissipation (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$P_D$	2.5 1.3	1.3 0.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150		$^\circ\text{C}$

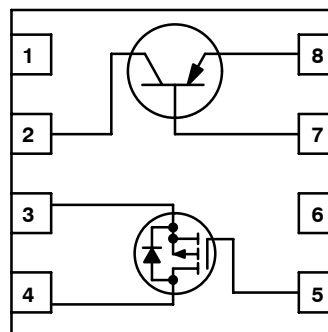
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

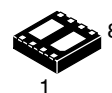


ON Semiconductor®

<http://onsemi.com>

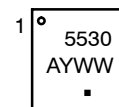


(Top View)



DFN8  
CASE 506AL

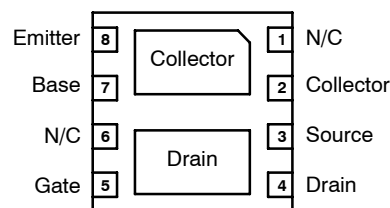
### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENT



(Bottom View)

### ORDERING INFORMATION

Device	Package	Shipping†
NUS5530MNR2G	DFN8 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NUS5530MN

## MAXIMUM RATINGS FOR PNP TRANSISTORS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	-35	Vdc
Collector-Base Voltage	$V_{CBO}$	-55	Vdc
Emitter-Base Voltage	$V_{EBO}$	-5.0	Vdc
Collector Current – Continuous	$I_C$	-2.0	Adc
Collector Current – Peak	$I_{CM}$	-7.0	A
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

## THERMAL CHARACTERISTICS FOR P-CHANNEL FET

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 4) $t \leq 5$ sec Steady State	$R_{\theta JA}$	40 80	50 95	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Foot (Drain) Steady State	$R_{\theta JF}$	15	20	$^\circ\text{C}/\text{W}$

## THERMAL CHARACTERISTICS FOR PNP TRANSISTORS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 1)	635 5.1	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	200	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 2)	1.35 11	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	90	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Lead #1	$R_{\theta JL}$	15	$^\circ\text{C}/\text{W}$
Total Device Dissipation (Single Pulse < 10 sec)	$P_{D\text{single}}$ (Notes 2 & 3)	2.75	W
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ 100 mm<sup>2</sup>, 1 oz copper traces.
2. FR-4 @ 500 mm<sup>2</sup>, 1 oz copper traces.
3. Thermal response.

# NUS5530MN

## ELECTRICAL CHARACTERISTICS FOR P-CHANNEL FET ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.6		-1.2	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1.0	$\mu\text{A}$
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$			-5.0	
On-State Drain Current (Note 5)	$I_{D(on)}$	$V_{DS} \leq -5.0 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20			A
Drain-Source On-State Resistance (Note 5)	$r_{DS(on)}$	$V_{GS} = -3.6 \text{ V}, I_D = -1.0 \text{ A}$	-	0.050	0.06	$\Omega$
		$V_{GS} = -2.5 \text{ V}, I_D = -1.0 \text{ A}$		0.070	0.083	
Forward Transconductance (Note 5)	$g_{fs}$	$V_{DS} = -10 \text{ V}, I_D = -3.9 \text{ A}$		12		Mhos
Diode Forward Voltage (Note 5)	$V_{SD}$	$I_S = -2.1 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8	-1.2	V

### Dynamic (Note 6)

Total Gate Charge	$Q_G$	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.9 \text{ A}$		9.7	22	nC
Gate-Source Charge	$Q_{GS}$			1.2		
Gate-Drain Charge	$Q_{GD}$			3.6		
Input Capacitance	$C_{iss}$	$V_{DS} = -5.0 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, f = 1.0 \text{ MHz}$		710		pF
Output Capacitance	$C_{oss}$			400		
Reverse Transfer Capacitance	$C_{rss}$			140		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, R_L = 10 \Omega, I_D \cong -1.0 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$		14	30	ns
Rise Time	$t_r$			22	55	
Turn-Off Delay Time	$t_{d(off)}$			42	100	
Fall Time	$t_f$			35	70	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -1.1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		30	60	

4. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

5. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

6. Guaranteed by design, not subject to production testing.

# NUS5530MN

## ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTORS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector - Emitter Breakdown Voltage ( $I_C = -10 \text{ mAdc}$ , $I_B = 0$ )	$V_{(BR)CEO}$	-35	-45	-	Vdc
Collector - Base Breakdown Voltage ( $I_C = -0.1 \text{ mAdc}$ , $I_E = 0$ )	$V_{(BR)CBO}$	-55	-65	-	Vdc
Emitter - Base Breakdown Voltage ( $I_E = -0.1 \text{ mAdc}$ , $I_C = 0$ )	$V_{(BR)EBO}$	-5.0	-7.0	-	Vdc
Collector Cutoff Current ( $V_{CB} = -35 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	-	-0.03	-0.1	$\mu\text{Adc}$
Collector - Emitter Cutoff Current ( $V_{CES} = -35 \text{ Vdc}$ )	$I_{CES}$	-	-0.03	-0.1	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{EB} = -6.0 \text{ Vdc}$ )	$I_{EBO}$	-	-0.01	-0.1	$\mu\text{Adc}$
<b>ON CHARACTERISTICS</b>					
DC Current Gain (Note 7) ( $I_C = -1.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = -1.5 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = -2.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ )	$h_{FE}$	100 100 100	200 200 200	- 400 -	
Collector - Emitter Saturation Voltage (Note 7) ( $I_C = -0.1 \text{ A}$ , $I_B = -0.010 \text{ A}$ ) ( $I_C = -1.0 \text{ A}$ , $I_B = -0.010 \text{ A}$ ) ( $I_C = -2.0 \text{ A}$ , $I_B = -0.02 \text{ A}$ )	$V_{CE(sat)}$	- - -	- - -	-0.10 -0.15 -0.30	V
Base - Emitter Saturation Voltage (Note 7) ( $I_C = -1.0 \text{ A}$ , $I_B = -0.01 \text{ A}$ )	$V_{BE(sat)}$	-	-0.68	-0.85	V
Base - Emitter Turn-on Voltage (Note 7) ( $I_C = -2.0 \text{ A}$ , $V_{CE} = -3.0 \text{ V}$ )	$V_{BE(on)}$	-	-0.81	-0.875	V
Cutoff Frequency ( $I_C = -100 \text{ mA}$ , $V_{CE} = -5.0 \text{ V}$ , $f = 100 \text{ MHz}$ )	$f_T$	100	-	-	MHz
Input Capacitance ( $V_{EB} = -0.5 \text{ V}$ , $f = 1.0 \text{ MHz}$ )	$C_{ibo}$	-	600	650	pF
Output Capacitance ( $V_{CB} = -3.0 \text{ V}$ , $f = 1.0 \text{ MHz}$ )	$C_{obo}$	-	85	100	pF
Turn-on Time ( $V_{CC} = -10 \text{ V}$ , $I_{B1} = -100 \text{ mA}$ , $I_C = -1 \text{ A}$ , $R_L = 3 \Omega$ )	$t_{on}$	-	35	-	nS
Turn-off Time ( $V_{CC} = -10 \text{ V}$ , $I_{B1} = I_{B2} = -100 \text{ mA}$ , $I_C = 1 \text{ A}$ , $R_L = 3 \Omega$ )	$t_{off}$	-	225	-	nS

7. Pulsed Condition: Pulse Width = 300  $\mu\text{sec}$ , Duty Cycle  $\leq 2\%$

TYPICAL ELECTRICAL CHARACTERISTICS FOR P-CHANNEL FET

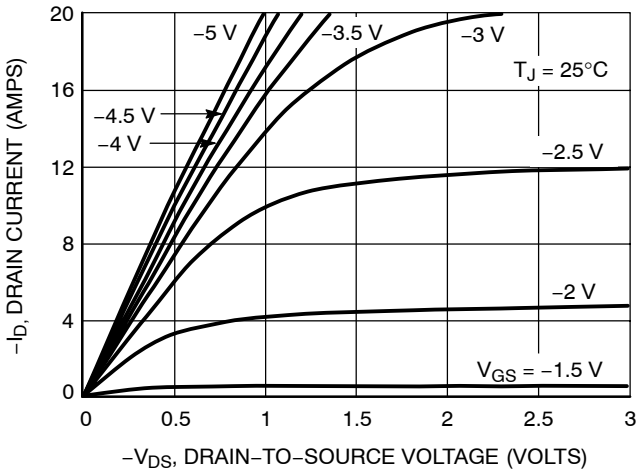


Figure 1. On-Region Characteristics

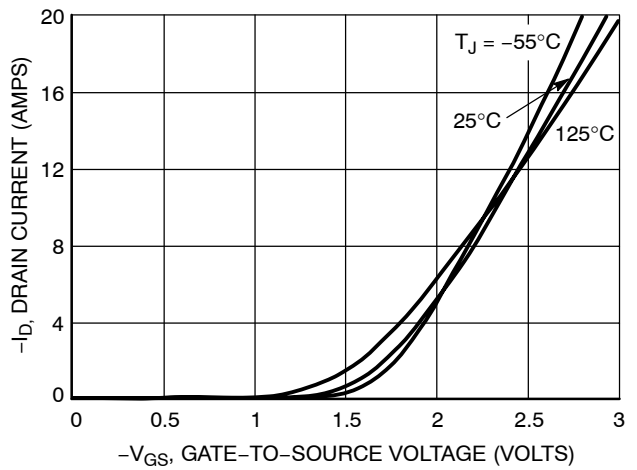


Figure 2. Transfer Characteristics

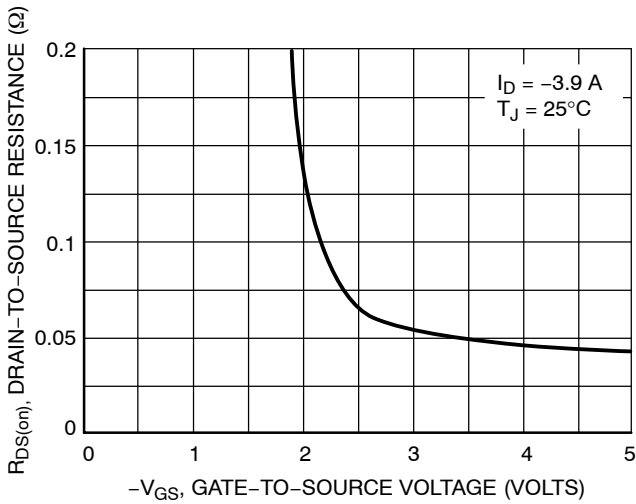


Figure 3. On-Resistance versus Gate-to-Source Voltage

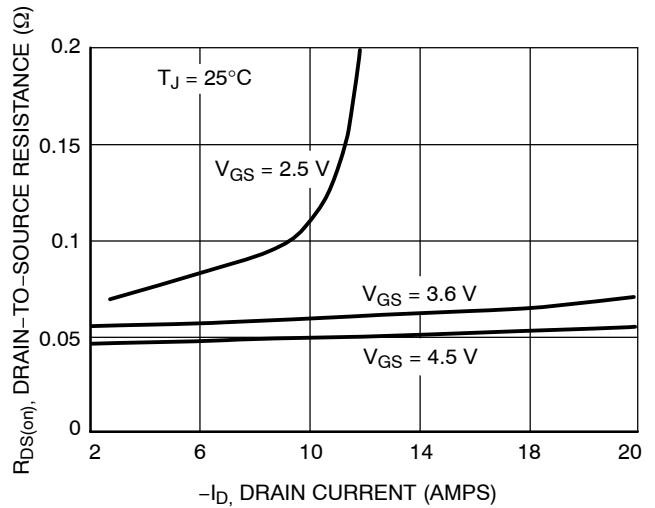


Figure 4. On-Resistance versus Drain Current and Gate Voltage

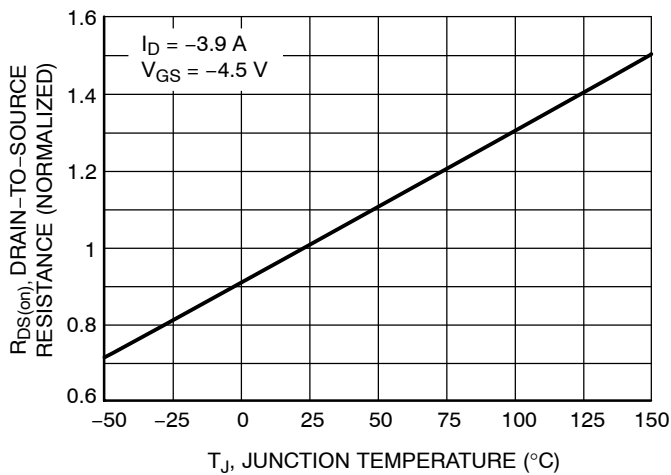


Figure 5. On-Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS FOR P-CHANNEL FET

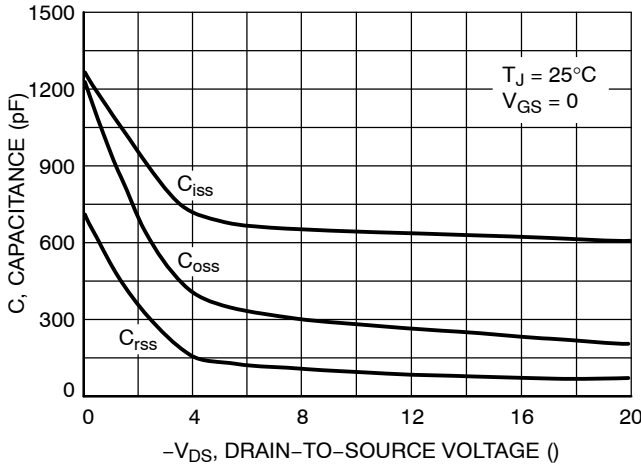


Figure 6. Capacitance Variation

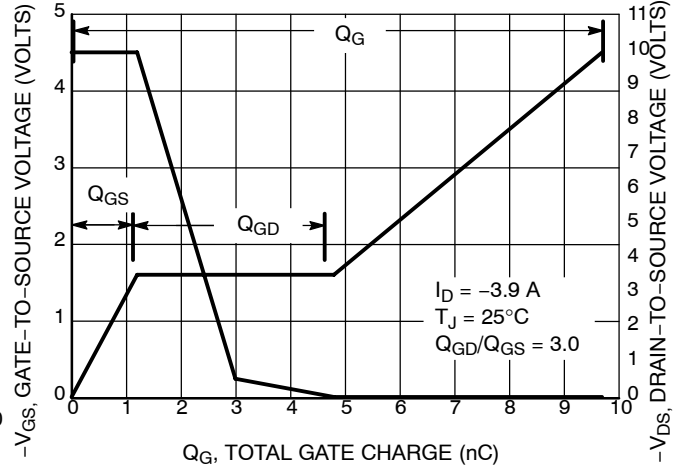


Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

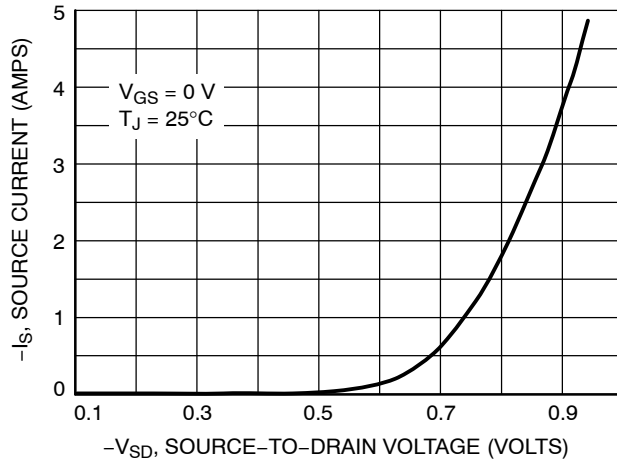


Figure 8. Diode Forward Voltage versus Current

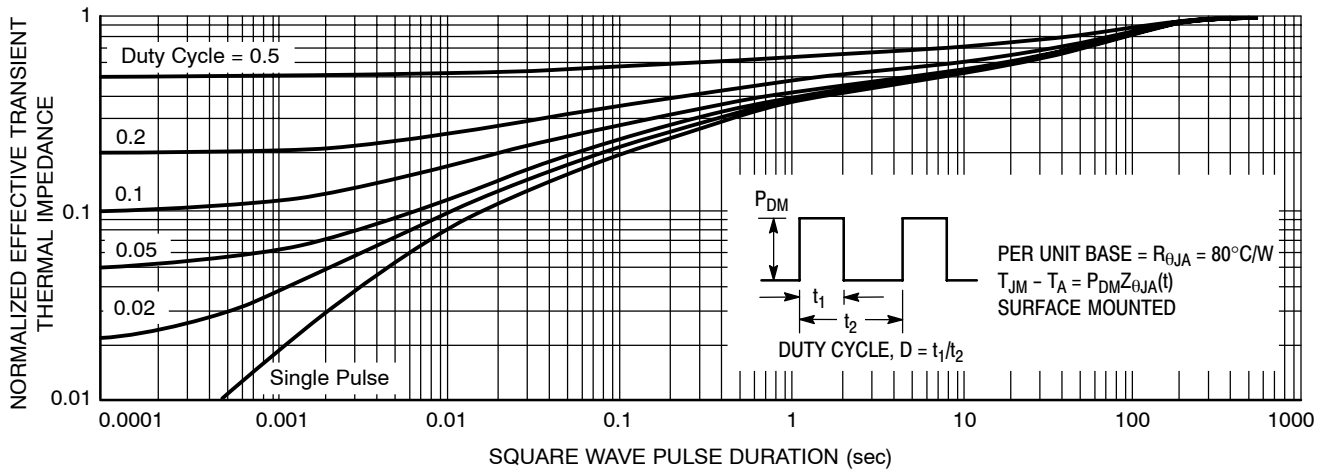


Figure 9. Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTOR

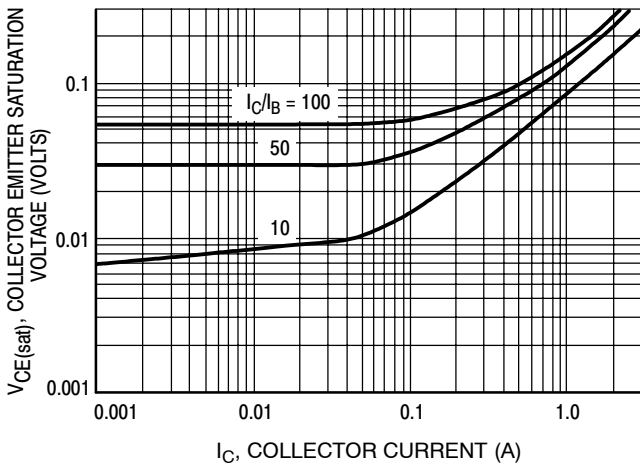


Figure 10. Collector Emitter Saturation Voltage versus Collector Current

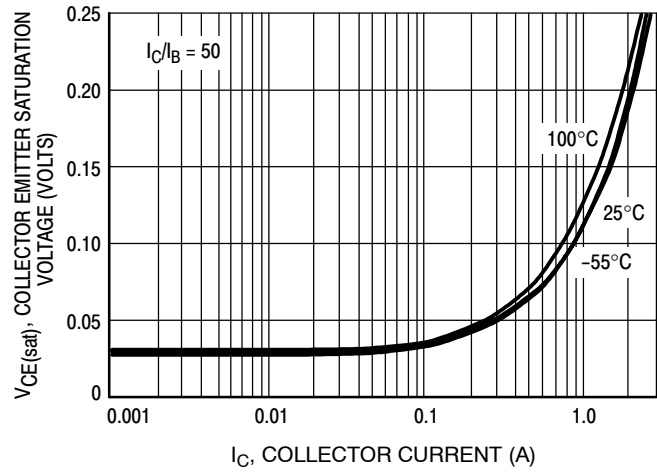


Figure 11. Collector Emitter Saturation Voltage versus Collector Current

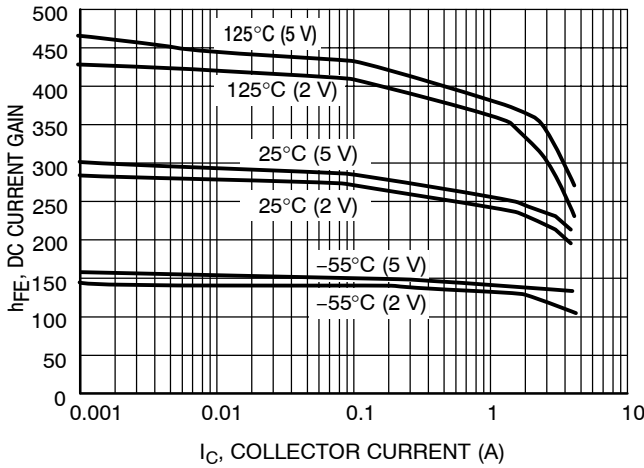


Figure 12. DC Current Gain versus Collector Current

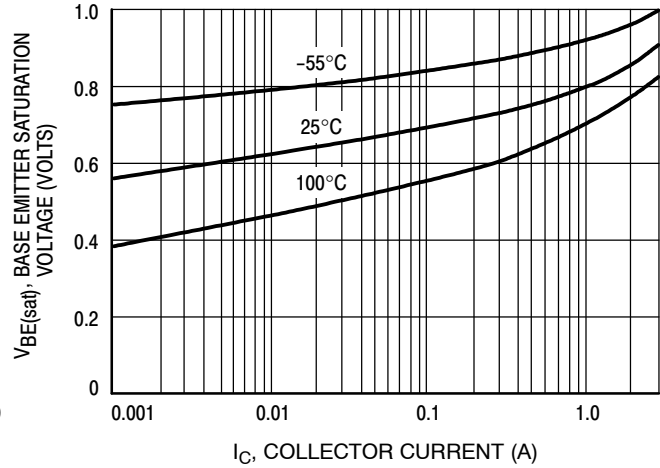


Figure 13. Base Emitter Saturation Voltage versus Collector Current

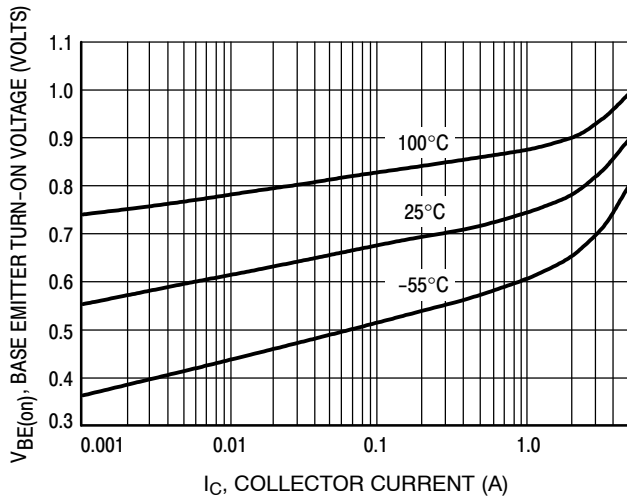


Figure 14. Base Emitter Turn-On Voltage versus Collector Current

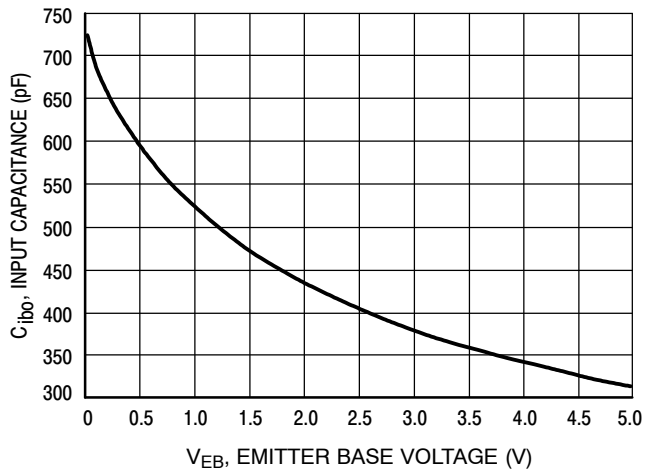


Figure 15. Input Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS FOR PNP TRANSISTOR

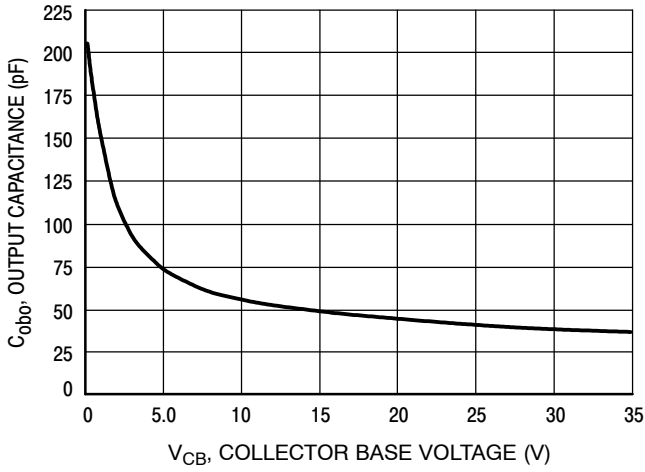


Figure 16. Output Capacitance

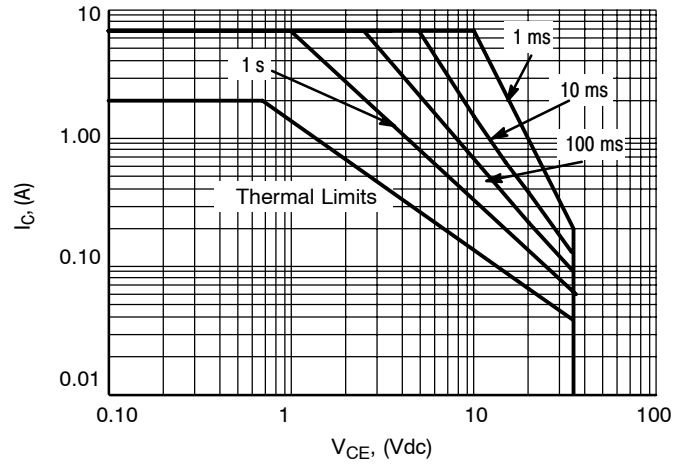


Figure 17. Safe Operating Area

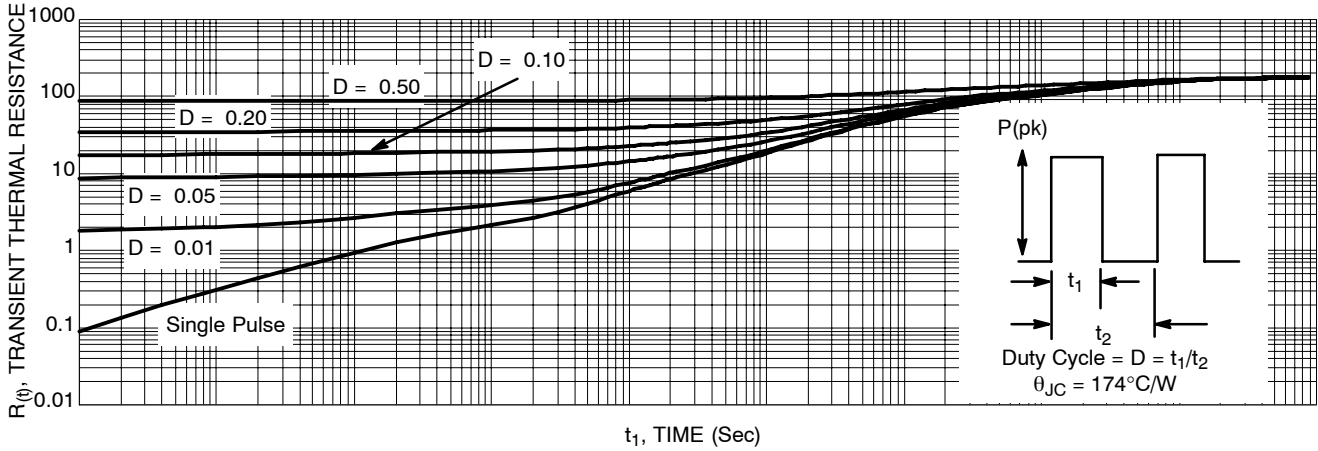


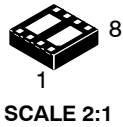
Figure 18. Normalized Thermal Response



# MECHANICAL CASE OUTLINE

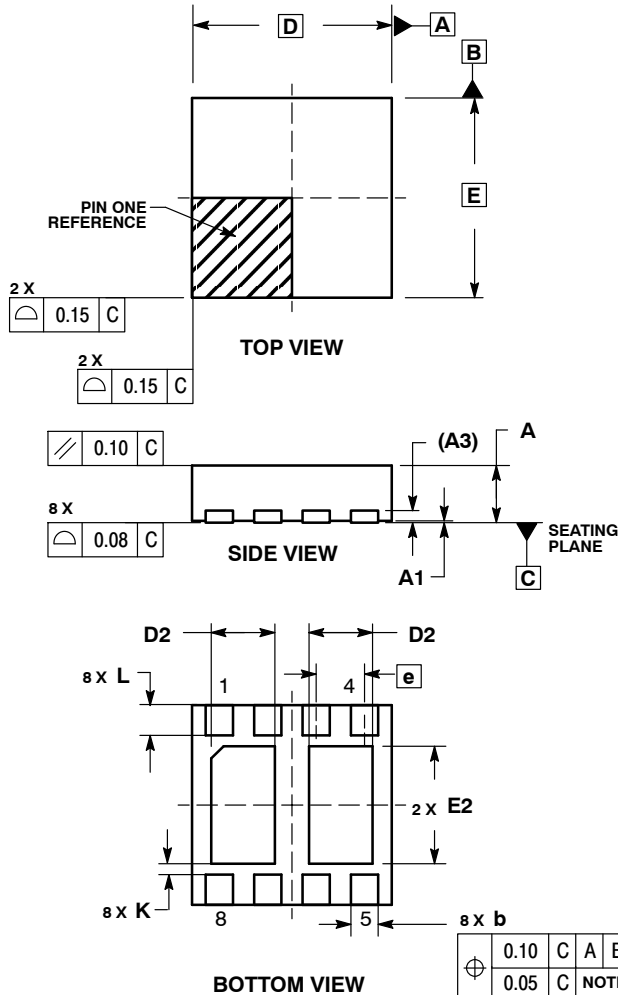
## PACKAGE DIMENSIONS

ON Semiconductor®



**DFN8**  
CASE 506AL-01  
ISSUE A

DATE 20 DEC 2005

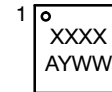


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.35	0.40	0.45
D	3.30 BSC		
D2	0.95	1.05	1.15
E	3.30 BSC		
E2	1.80	1.90	2.00
e	0.80 BSC		
K	0.21	---	---
L	0.30	0.40	0.50

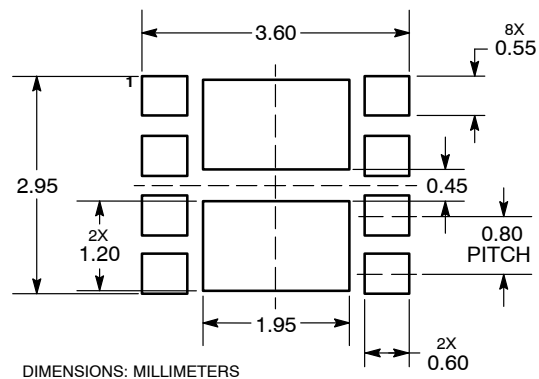
**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking.  
 Pb-Free indicator, "G" or microdot "•", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON20636D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DFN8, 3.3X3.3 MM, 0.8 MM PITCH, DUAL FLAG</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative