NTZD5110N

MOSFET – Dual, N-Channel with ESD Protection, Small Signal, SOT-563
60 V, 310 mA

Features
- Low $R_{DS(on)}$ Improving System Efficiency
- Low Threshold Voltage
- ESD Protected Gate
- Small Footprint 1.6 x 1.6 mm
- These are Pb−Free Devices

Applications
- Load/Power Switches
- Driver Circuits: Relays, Lamps, Displays, Memories, etc.
- Battery Management/Battery Operated Systems
- Cell Phones, Digital Cameras, PDAs, Pagers, etc.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	294	mA
		T_A = 85°C		212	
Power Dissipation (Note 1)	Steady State		P_D	250	mW
Continuous Drain Current (Note 1)	t ≤ 5 s	T_A = 25°C	I_D	310	mA
		T_A = 85°C		225	
Power Dissipation (Note 1)	t ≤ 5 s		P_D	280	mW
Pulsed Drain Current	t_p = 10 μs		I_{DM}	590	mA
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	350	mA
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C
Gate−Source ESD Rating (HBM, Method 3015)			ESD	1800	V

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	500	°C/W
Junction−to−Ambient – t ≤ 5 s (Note 1)		447	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu. area = 1.127 in sq [1 oz] including traces).

ON Semiconductor®

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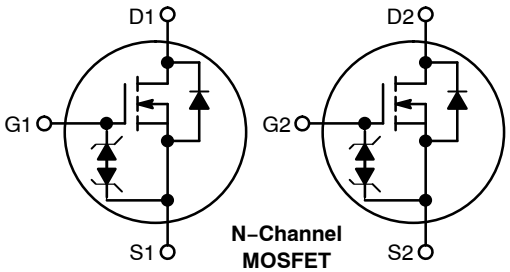
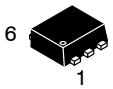
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D Max
60	1.6 Ω @ 10 V	310 mA
	2.5 Ω @ 4.5 V	



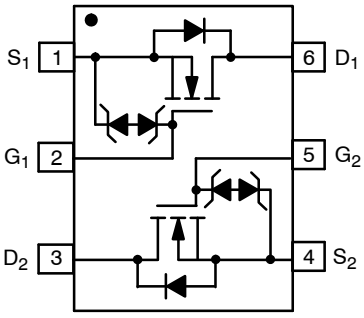


SOT−563
CASE 463A

MARKING DIAGRAM

S7 = Specific Device Code
M = Date Code
(Note: Microdot may be in either location)

PINOUT: SOT−563



Top View

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	–		–	71	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C	–	–	1.0	μA
			T_J = 125°C	–	–	500	
		V_{GS} = 0 V, V_{DS} = 50 V	T_J = 25°C	–	–	100	nA
			T_J = 85°C	–	–	100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		–	–	±10	μA
		V_{DS} = 0 V, V_{GS} = ±10 V		–	–	450	nA
		V_{DS} = 0 V, V_{GS} = ±5.0 V		–	–	150	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0	–	2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	–		–	4.0	–	mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 500 mA		–	1.19	1.6	Ω
		V_{GS} = 4.5 V, I_D = 200 mA		–	1.33	2.5	
Forward Transconductance	g_{FS}	V_{DS} = 5.0 V, I_D = 200 mA		–	80	–	S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 20 V		–	24.5	–	pF
Output Capacitance	C_{OSS}			–	4.2	–	
Reverse Transfer Capacitance	C_{RSS}			–	2.2	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V; I_D = 200 mA		–	0.7	–	nC
Threshold Gate Charge	$Q_{G(TH)}$			–	0.1	–	
Gate−to−Source Charge	Q_{GS}			–	0.3	–	
Gate−to−Drain Charge	Q_{GD}			–	0.1	–	
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 30 V, I_D = 200 mA, R_G = 10 Ω		–	12	–	ns
Rise Time	t_r			–	7.3	–	
Turn−Off Delay Time	$t_{d(OFF)}$			–	63.7	–	
Fall Time	t_f			–	30.6	–	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 200 mA	T_J = 25°C	–	0.8	1.2	V
			T_J = 85°C	–	0.7	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surface−mounted on FR4 board using 1 in. sq. pad size (Cu. area = 1.127 in sq [1 oz] including traces).
3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

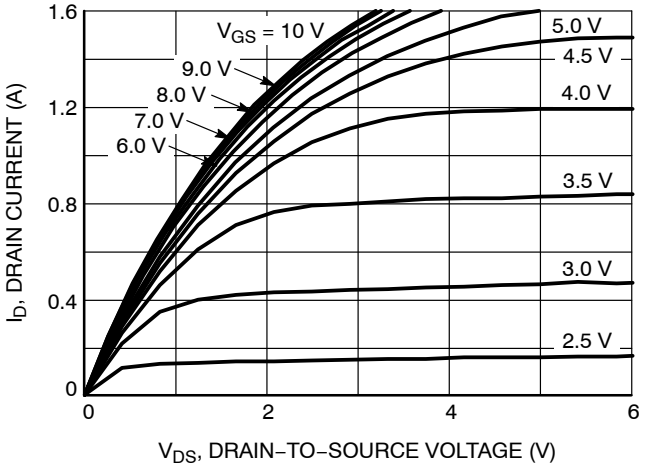


Figure 1. On−Region Characteristics

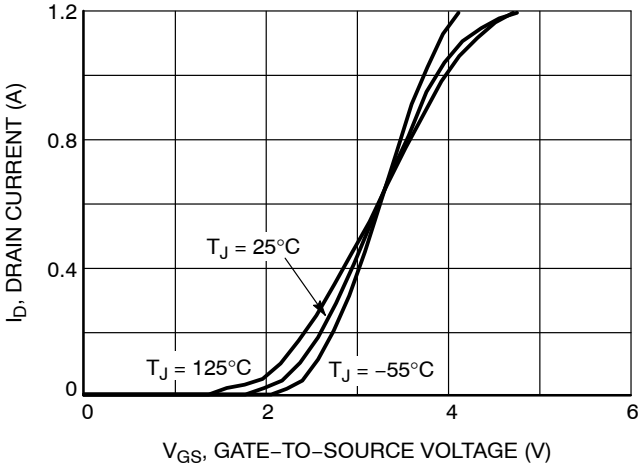


Figure 2. Transfer Characteristics

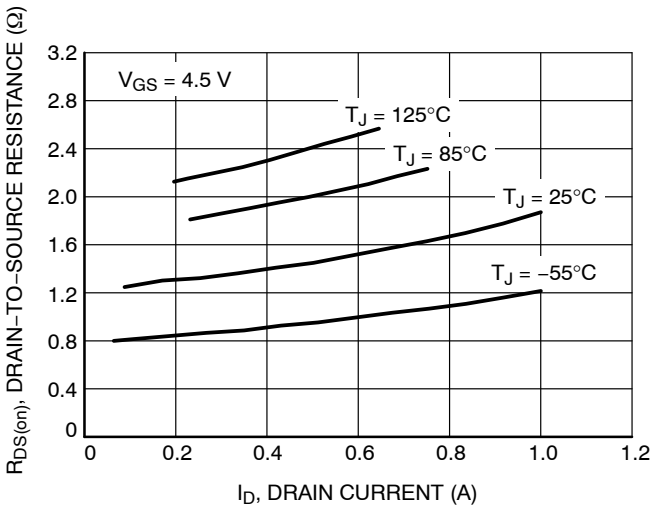


Figure 3. On−Resistance vs. Drain Current and Temperature

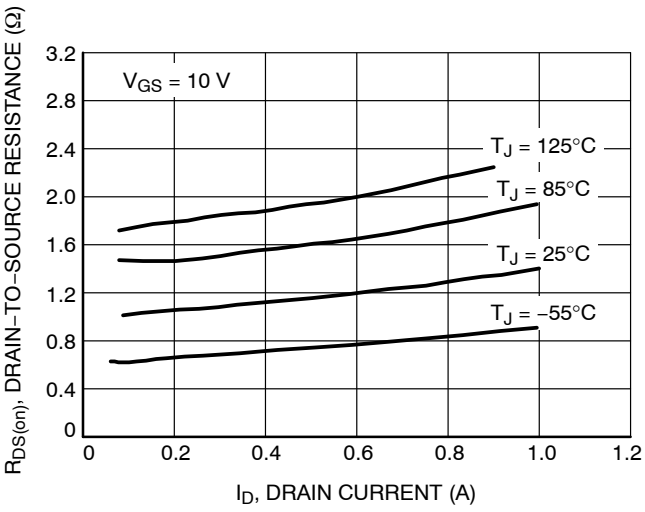


Figure 4. On−Resistance vs. Drain Current and Temperature

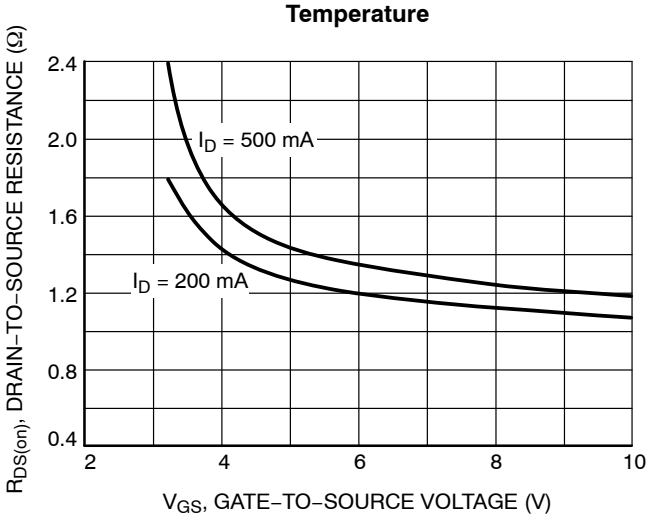


Figure 5. On−Resistance vs. Gate−to−Source Voltage

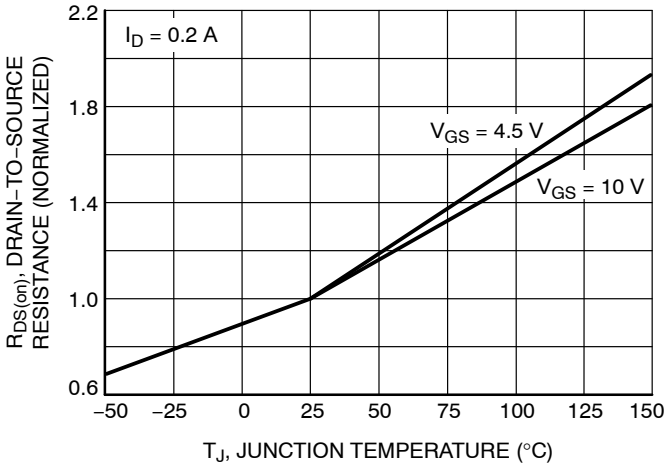


Figure 6. On−Resistance Variation with Temperature

TYPICAL CHARACTERISTICS

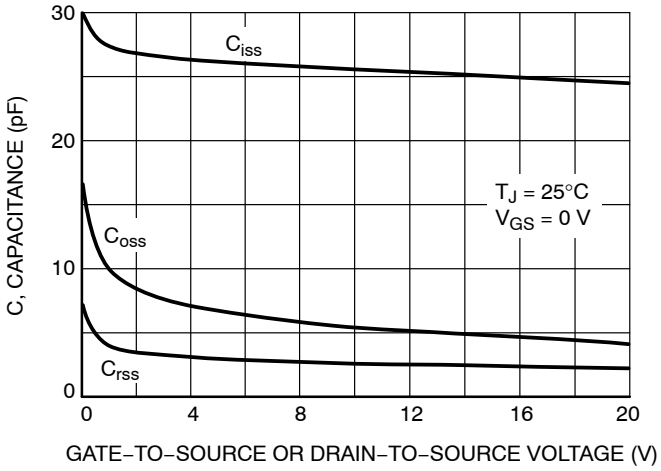


Figure 7. Capacitance Variation

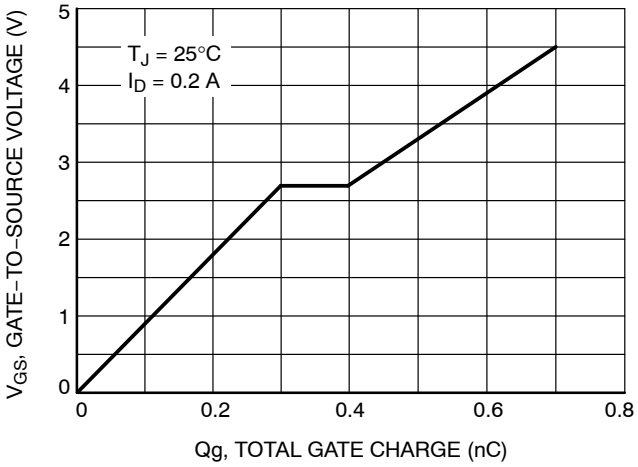


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

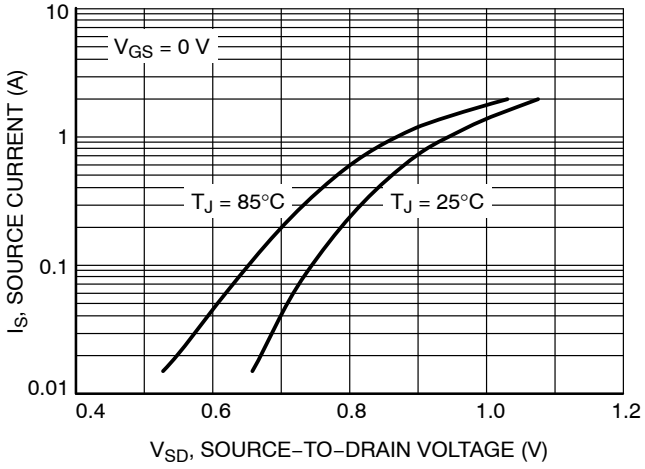
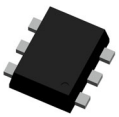


Figure 9. Diode Forward Voltage vs. Current

ORDERING INFORMATION

Device	Package	Shipping
NTZD5110NT1G	SOT−563 (Pb−Free)	4000 / Tape & Reel
NTZD5110NT5G	SOT−563 (Pb−Free)	8000 / Tape & Reel

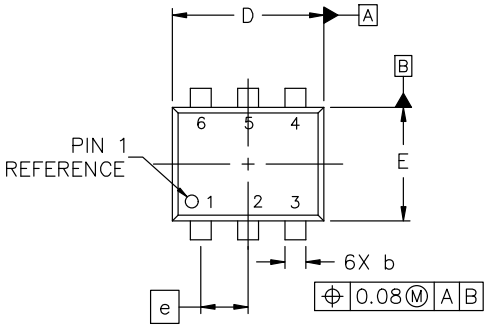
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



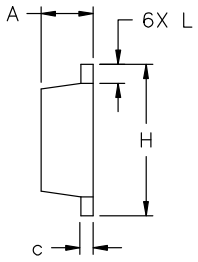
SOT−563−6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

DATE 15 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

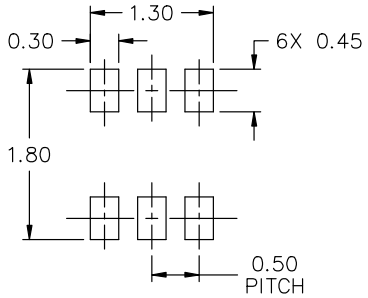


TOP VIEW



SIDE VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

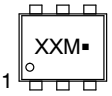
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−563−6 1.60x1.20x0.55, 0.50P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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