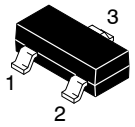
MOSFET – Single P-Channel, Small Signal, SOT-23

-8.0 V, -3.7 A

NTR2101P

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
−8.0 V	39 mΩ @ −4.5 V	−3.7 A
	52 mΩ @ −2.5 V	
	79 mΩ @ −1.8 V	



SOT−23
CASE 318
STYLE 21

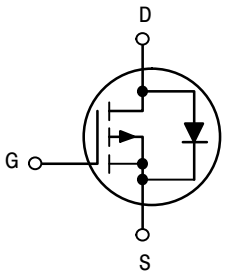
Features

- Leading Trench Technology for Low $R_{DS(on)}$
- −1.8 V Rated for Low Voltage Gate Drive
- SOT−23 Surface Mount for Small Footprint (3 x 3 mm)
- This is a Pb−Free Device

Applications

- High Side Load Switch
- DC−DC Conversion
- Cell Phone, Notebook, PDAs, etc.

P−Channel



MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain−to−Source Voltage			−8.0	V
V_{GS}	Gate−to−Source Voltage			±8.0	V
I_D	Continuous Drain Current (Note 1)	t ≤ 5 s	T_A = 25°C	−3.7	A
			T_A = 70°C	−3.0	
P_D	Power Dissipation (Note 1)	t ≤ 5 s		0.96	W
I_{DM}	Pulsed Drain Current	t_p = 10 μs		−11	A
T_J, T_{STG}	Operating Junction and Storage Temperature			−55 to 150	°C
I_S	Source Current (Body Diode)			−1.2	A
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

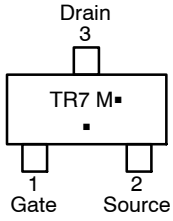
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State	$R_{\theta JA}$	160	°C/W
Junction−to−Ambient − t ≤ 5 s	$R_{\theta JA}$	130	

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

MARKING DIAGRAM & PIN ASSIGNMENT



TR7 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NTR2101PT1G	SOT−23 (Pb−Free)	3,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA		−8.0			V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient				10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = −6.4 V	T_J = 25°C			−1.0	μA
			T_J = 125°C			−100	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±8.0 V				±100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA		−0.40		−1.0	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient				2.7		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = −4.5 V, I_D = −3.5 A			39	52	mΩ
		V_{GS} = −2.5 V, I_D = −3.0 A			52	72	
		V_{GS} = −1.8 V, I_D = −2.0 A			79	120	
g_{FS}	Forward Transconductance	V_{GS} = −5.0 V, I_D = −3.5 A			9.0		S
CHARGES AND CAPACITANCES							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −4.0 V			1173		pF
C_{OSS}	Output Capacitance				289		
C_{RSS}	Reverse Transfer Capacitance				218		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = −4.5 V, V_{DS} = −4.0 V, I_D = −3.5 A			12	15	nC
Q_{GS}	Gate−to−Source Charge				3.8		
Q_{GD}	Gate−to−Drain Charge				2.5		
SWITCHING CHARACTERISTICS (Note 3)							
$t_{d(on)}$	Turn−On Delay Time	V_{GS} = −4.5 V, V_{DD} = −4.0 V, I_D = −1.2 A, R_G = 6.0 Ω			7.4	15	ns
t_r	Rise Time				15.75	25	
$t_{d(off)}$	Turn−Off Delay Time				38	58	
t_f	Fall Time				31	51	
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = −1.2 A	T_J = 25°C		−0.73	−1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

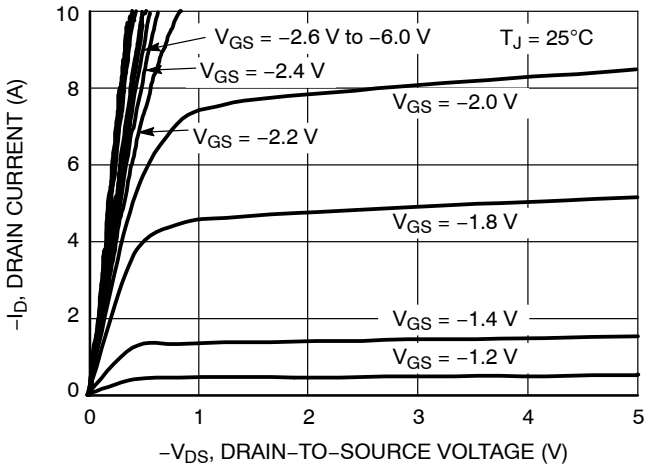


Figure 1. On−Region Characteristics

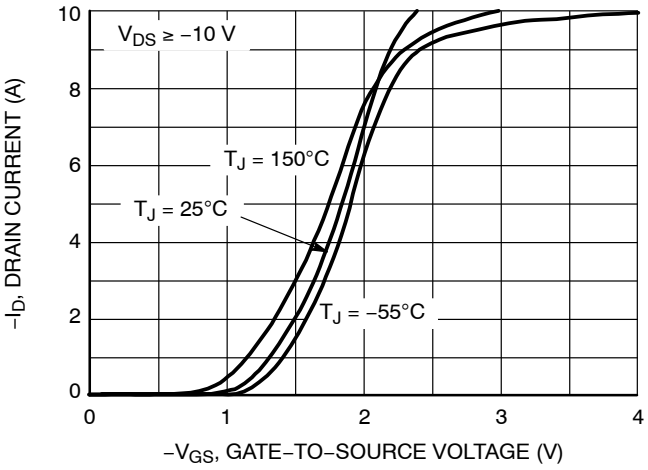


Figure 2. Transfer Characteristics

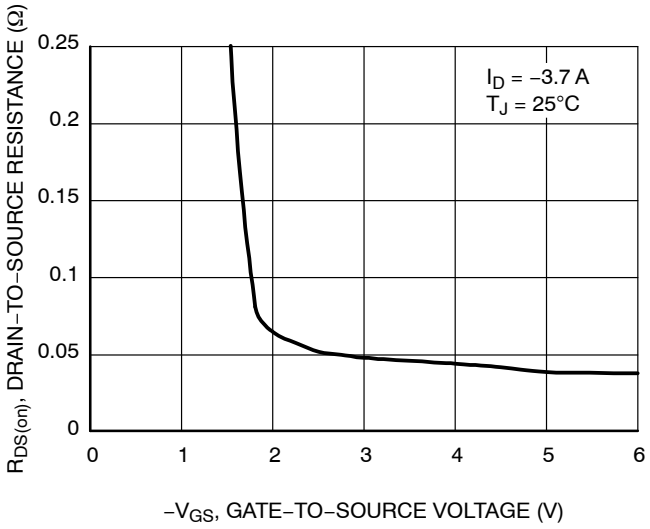


Figure 3. On−Resistance versus Gate−to−Source Voltage

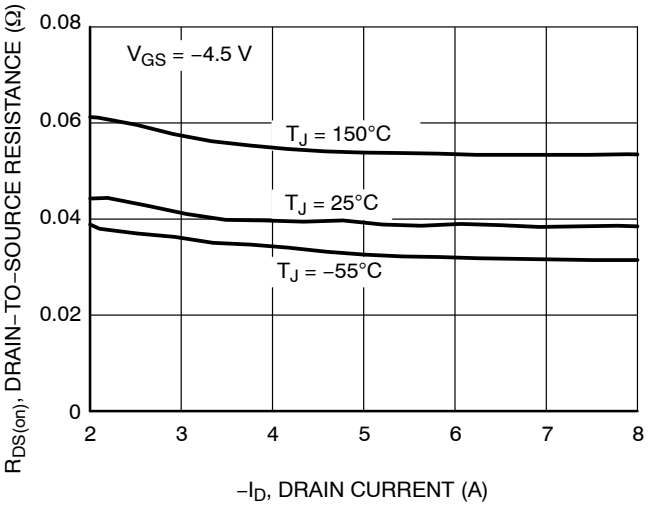


Figure 4. On−Resistance versus Drain Current and Gate Voltage

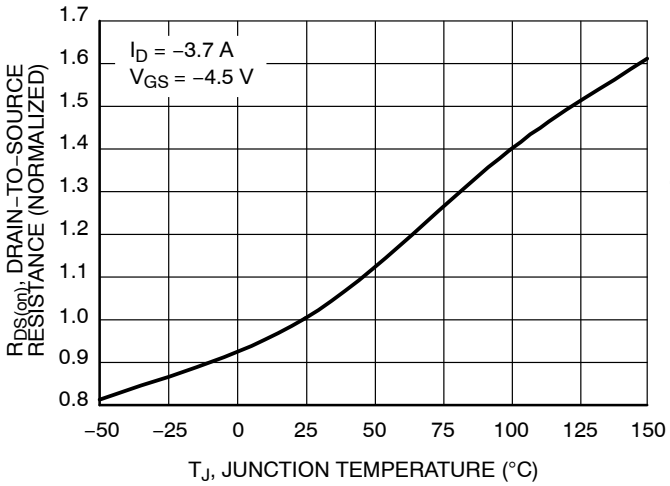


Figure 5. On−Resistance Variation with Temperature

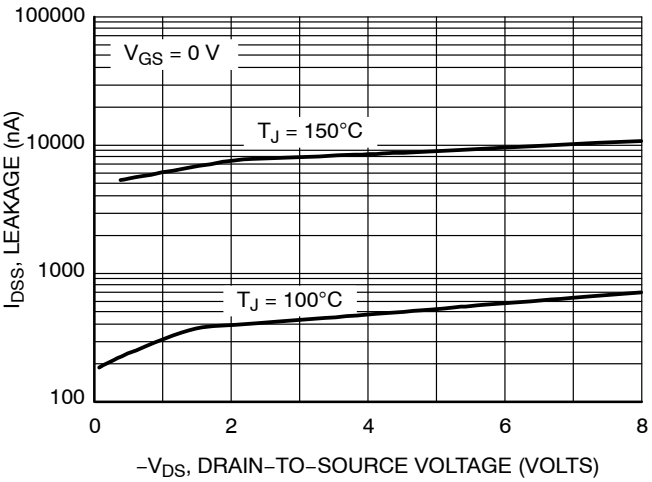


Figure 6. Drain−to−Source Leakage Current versus Voltage

TYPICAL CHARACTERISTICS (continued)

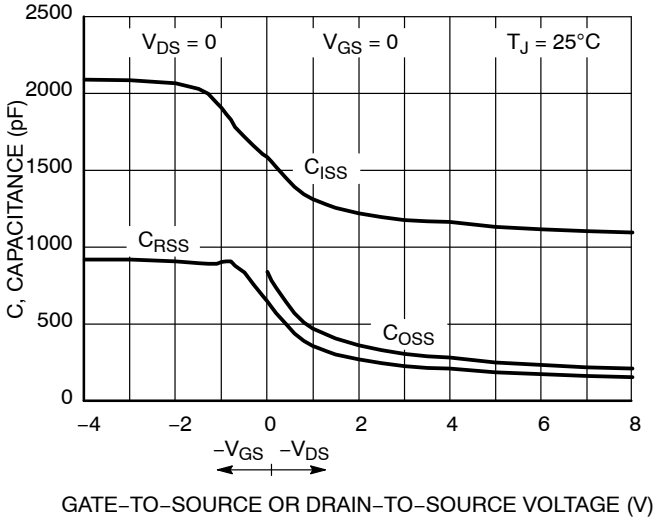


Figure 7. Capacitance Variation

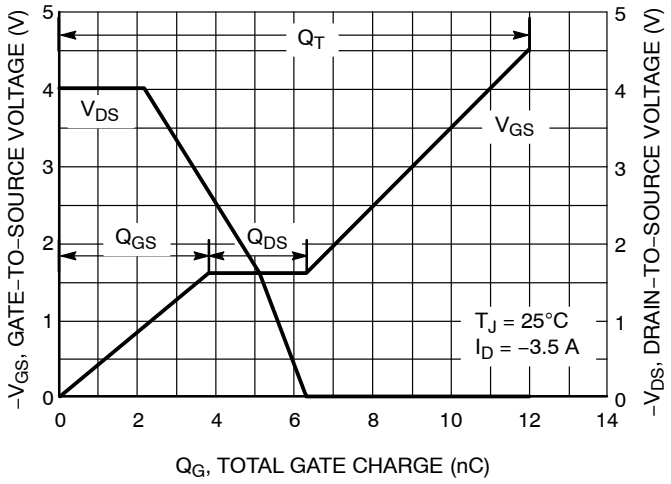


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

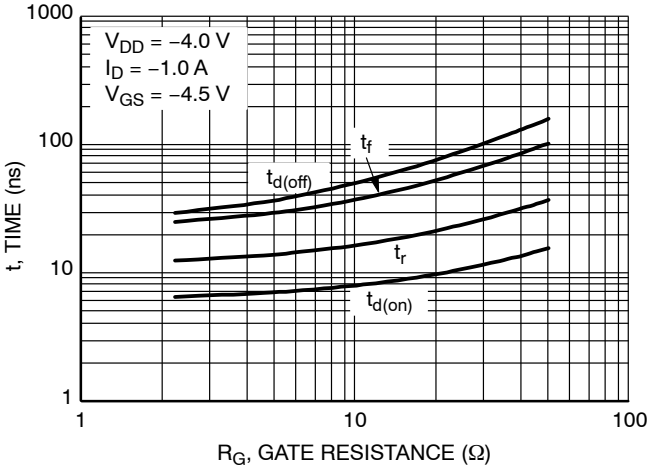


Figure 9. Resistive Switching Time Variation versus Gate Resistance

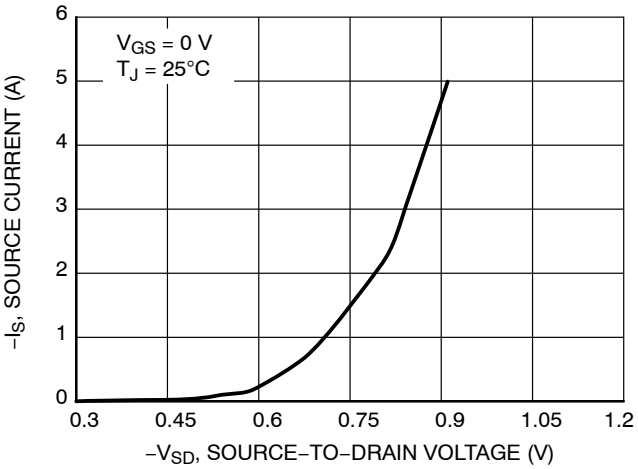


Figure 10. Diode Forward Voltage versus Current

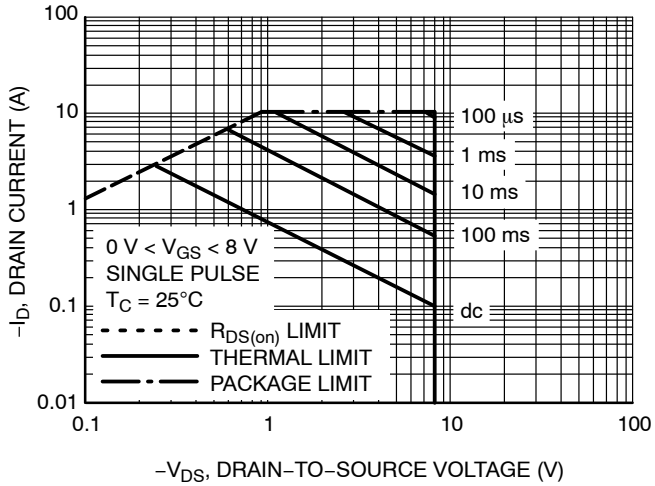


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS (continued)

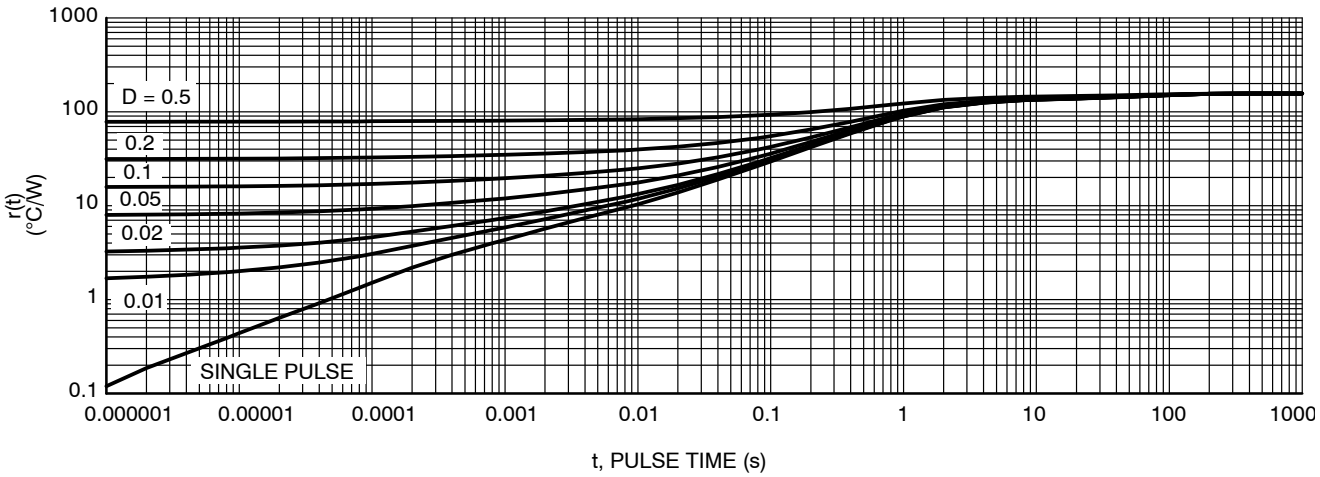
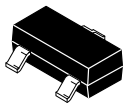


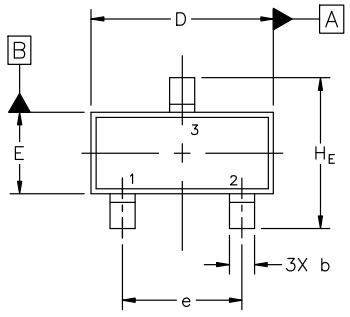
Figure 12. Thermal Response



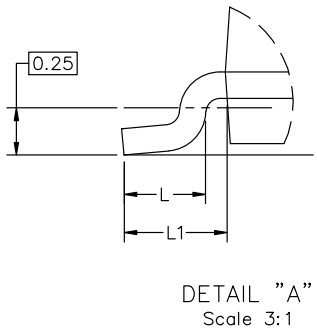
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

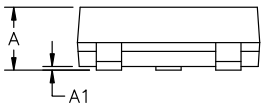
DATE 14 AUG 2024



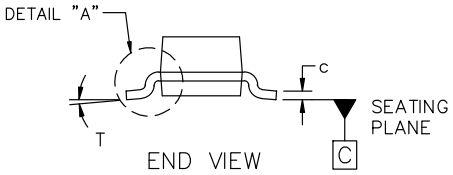
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

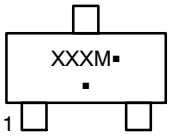


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

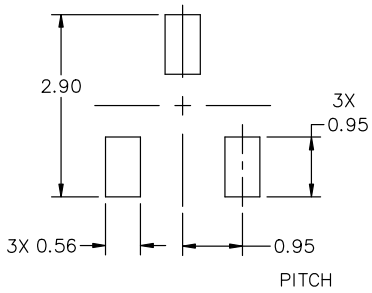
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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