MOSFET – Power, N-Channel, SUPERFET III, FRFET

650 V, 20 A, 190 mΩ

NTP190N65S3HF

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	190 mΩ @ 10 V	20 A

Description

SUPERFET III MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.
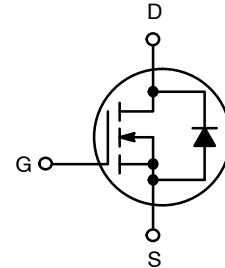
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 159 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 34 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 316 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

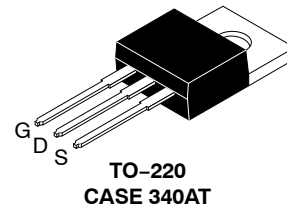### Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
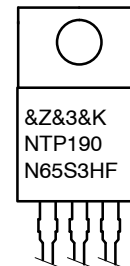- Industrial Power Supplies
- Lighting / Charger / Adapter

POWER MOSFET

TO−220
CASE 340AT

MARKING DIAGRAM

&Z&3&K
NTP190
N65S3HF

&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
NTP190N65S3HF	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current	– Continuous (T_C = 25°C)	20	A
		– Continuous (T_C = 100°C)	12.7	
I_{DM}	Drain Current	– Pulsed (Note 1)	50	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		220	mJ
I_{AS}	Avalanche Current (Note 2)		3.7	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		1.62	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	162	W
		– Derate Above 25°C	1.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 3.7 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 10 A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq$ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.77	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTP190N65S3HF	NTP190N65S3HF	TO−220	Tube	N/A	N/A	800 Units

NTP190N65S3HF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C		0.65		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			10	μA
		V_{DS} = 520 V, T_C = 125°C		65		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.43 mA	3.0		5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 10 A		159	190	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 10 A		11		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		1610		pF
C_{oss}	Output Capacitance			30		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		316		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		59		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 10 A, V_{GS} = 10 V (Note 4)		34		nC
Q_{gs}	Gate to Source Gate Charge			11		nC
Q_{gd}	Gate to Drain "Miller" Charge			13		nC
ESR	Equivalent Series Resistance	f = 1 MHz		6.8		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 10 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)		19		ns
t_r	Turn-On Rise Time			19		ns
$t_{d(off)}$	Turn-Off Delay Time			58		ns
t_f	Turn-Off Fall Time			14		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				20	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				50	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 10 A			1.3	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 10 A, dI_F/dt = 100 A/μs		80		ns
Q_{rr}	Reverse Recovery Charge			264		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Essentially independent of operating temperature typical characteristics.
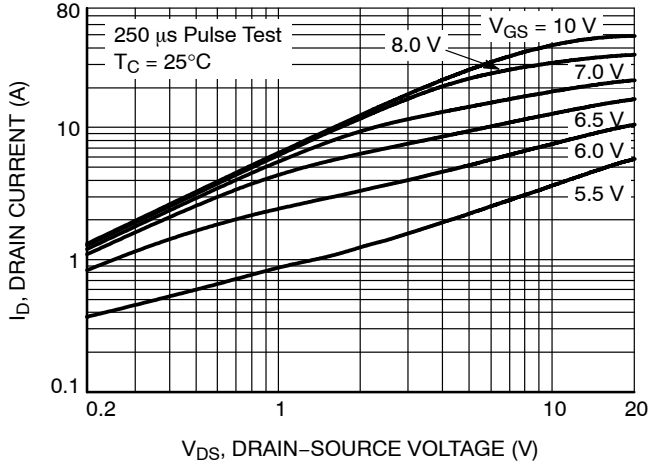
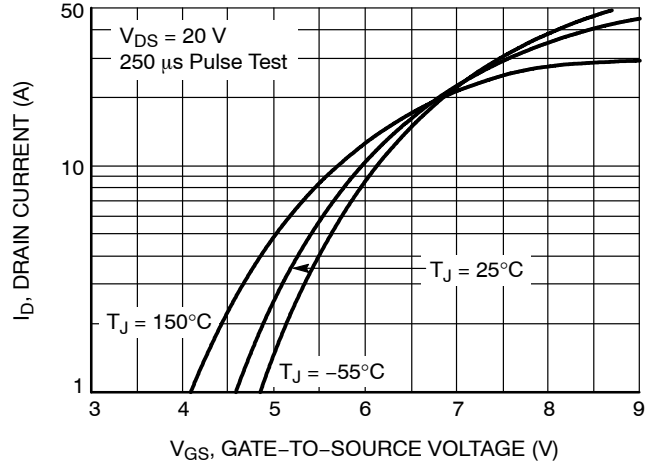## TYPICAL CHARACTERISTICS

Figure 1. On−Region Characteristics
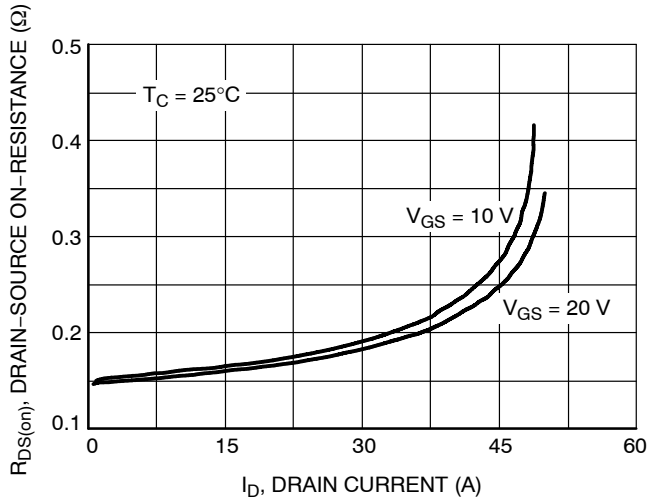

Figure 2. Transfer Characteristics

Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage
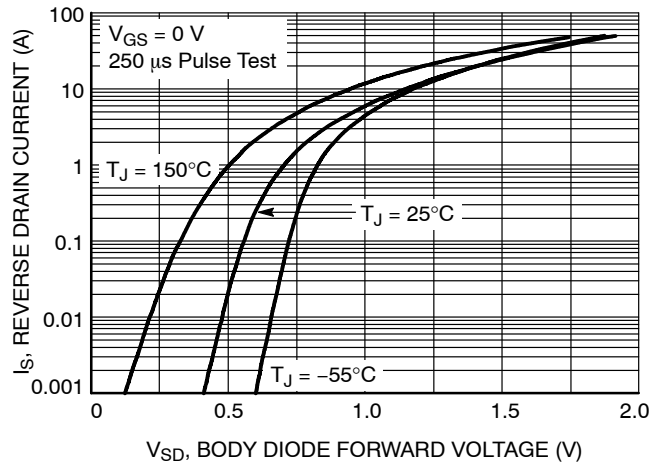

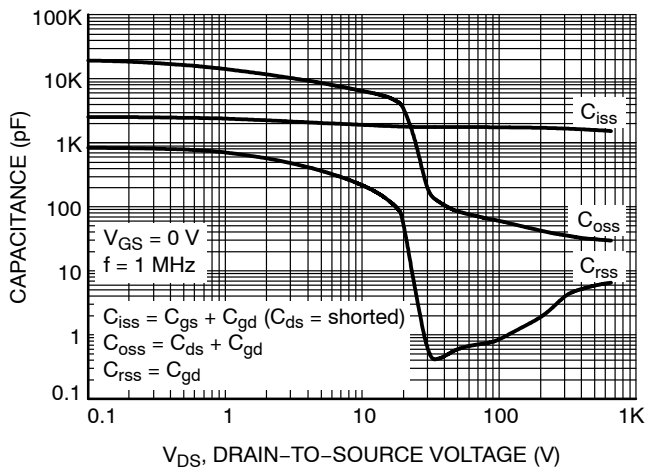**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**
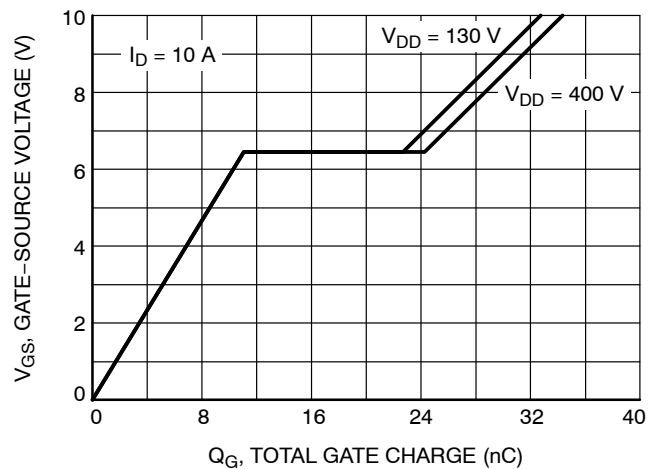

Figure 5. Capacitance Characteristics

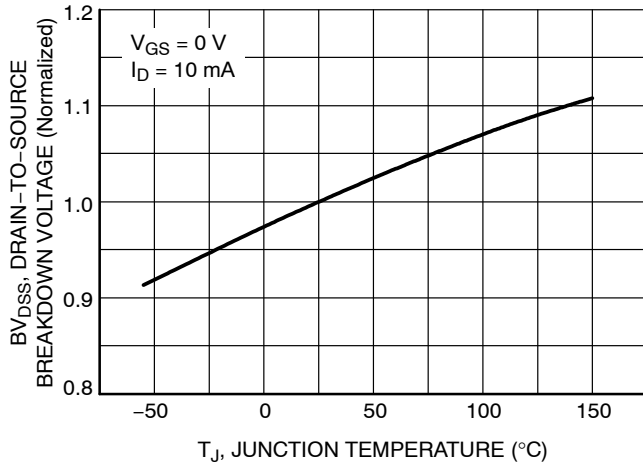**Figure 6. Gate Charge Characteristics**

TYPICAL CHARACTERISTICS
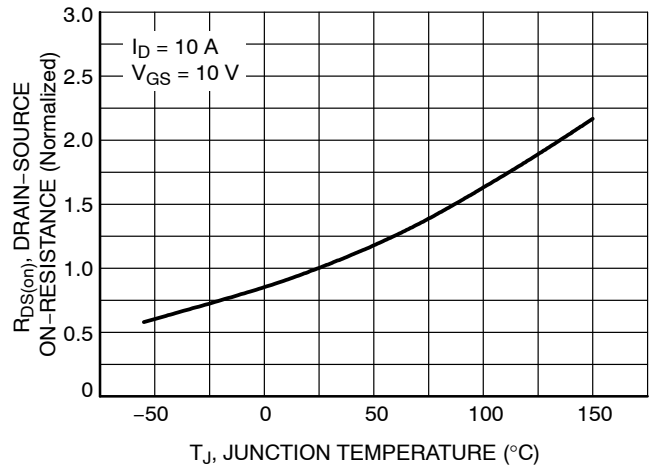

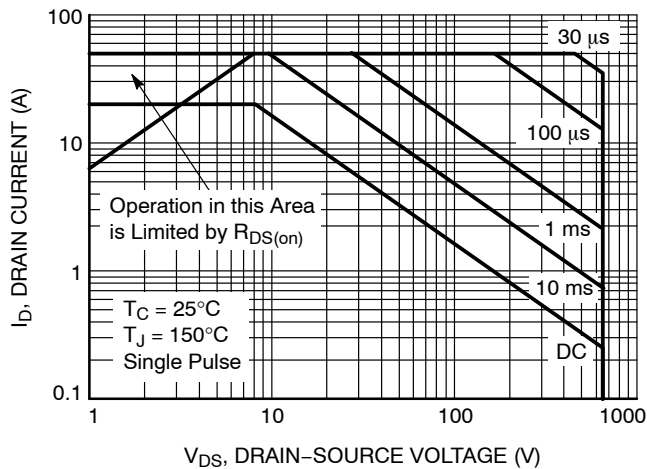**Figure 7. Breakdown Voltage Variation vs. Temperature**

Figure 8. On−Resistance Variation vs. Temperature

Figure 9. Maximum Safe Operating Area
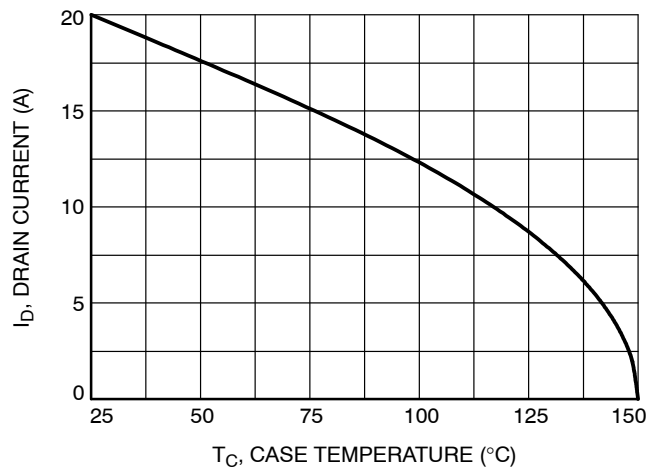
Figure 10. Maximum Drain Current vs. Case Temperature
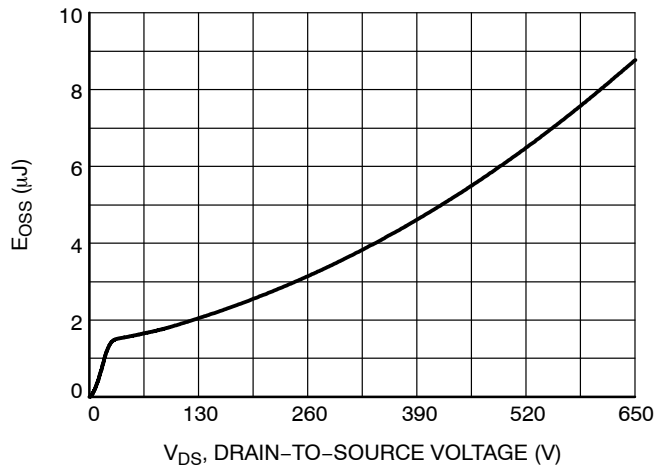
Figure 11. E$_{OSS}$ vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS
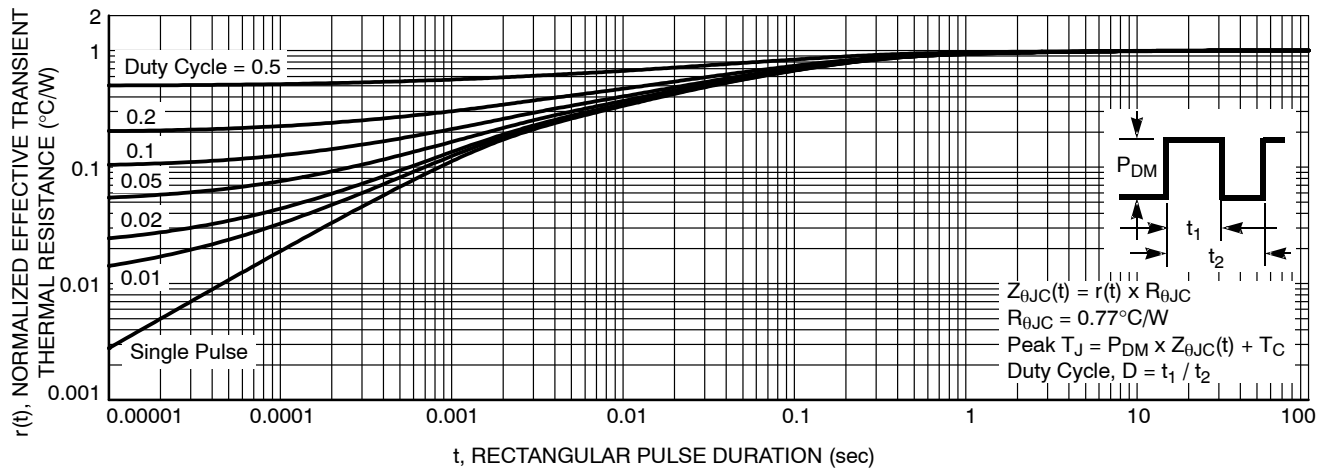
Figure 12. Transient Thermal Response Curve

Figure 13. Gate Charge Test Circuit & Waveform

Figure 14. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} \cdot L I_{AS}^{2}$$

Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms
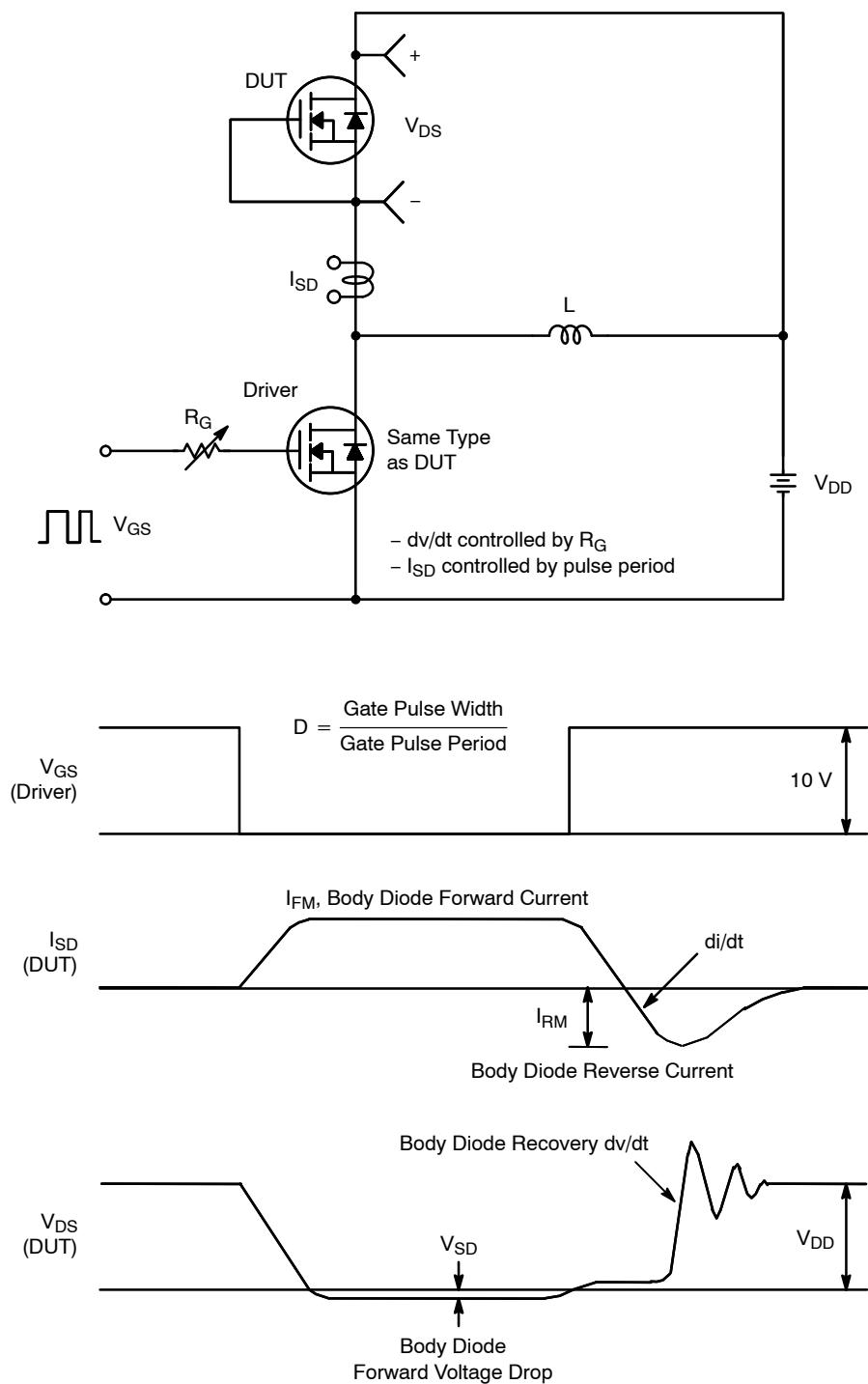
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

onsemi

TO−220−3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
Θ	3°	—	5°

SUPPLIER "A" PACKAGE SHAPE

SUPPLIER "B" PACKAGE SHAPE

IF PRESENT, SEE NOTE "D"

FRONT VIEWS

GENERIC MARKING DIAGRAM*
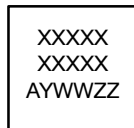
XXXXX
XXXXX
AYWWZZ

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

OPTIONAL CHAMFER

"A1" SEE NOTE "F"

NOTE "H"

SIDE VIEW

BACK VIEW

BOTTOM VIEW

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
   SINGLE GAUGE = 0.51 - 0.61
   DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	TO−220−3LD		PAGE 1 OF 1

ADDITIONAL INFORMATION

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