

MOSFET – Power, Single N-Channel

40 V, 52 A, 7.3 mΩ

NTMYS7D3N04CL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- LFAK4 Package, Industry Standard
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit	
V_{DSS}	Drain-to-Source Voltage	40	V	
V_{GS}	Gate-to-Source Voltage	± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady State $T_C = 25^\circ\text{C}$	52	A
		$T_C = 100^\circ\text{C}$	29	
P_D	Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)	$T_C = 25^\circ\text{C}$	38	W
		$T_C = 100^\circ\text{C}$	12	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State $T_A = 25^\circ\text{C}$	17	A
		$T_A = 100^\circ\text{C}$	12	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	$T_A = 25^\circ\text{C}$	3.8	W
		$T_A = 100^\circ\text{C}$	1.9	
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	269	A
T_J, T_{stg}	Operating Junction and Storage Temperature	-55 to +175		$^\circ\text{C}$
I_S	Source Current (Body Diode)	31		A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 2.9 \text{ A}$)	65		mJ
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 3)	4.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 3)	39	

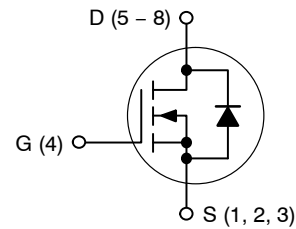
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	7.3 mΩ @ 10 V	52 A
	12 mΩ @ 4.5 V	

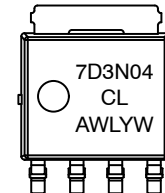


LFAK4
CASE 760AB

N-Channel



MARKING DIAGRAM



7D3N04CL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMYS7D3N04CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
V _{(BR)DSS} /T _J	Drain-to-Source Breakdown Voltage Temperature Coefficient			25		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 40 V			10	μA
					250	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 5)

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 30 μA	1.2		2.0	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 10 A		6.1	7.3	mΩ
		V _{GS} = 4.5 V, I _D = 10 A		9.7	12	
g _{FS}	Forward Transconductance	V _{DS} = 15 V, I _D = 10 A		33		S

CHARGES AND CAPACITANCES

C _{iss}	Input Capacitance	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		860		pF
C _{oss}	Output Capacitance			360		
C _{riss}	Reverse Transfer Capacitance			15		
Q _{G(TOT)}	Total Gate Charge	V _{GS} = 4.5 V, V _{DS} = 32 V, I _D = 10 A		7.0		nC
Q _{G(TH)}	Threshold Gate Charge	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 10 A		1.8		nC
Q _{GS}	Gate-to-Source Charge			3.3		
Q _{GD}	Gate-to-Drain Charge			2.5		
Q _{G(TOT)}	Total Gate Charge		V _{GS} = 10 V, V _{DS} = 32 V, I _D = 10 A		16	

SWITCHING CHARACTERISTICS (Note 6)

t _{d(on)}	Turn-On Delay Time	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 10 A, R _G = 1 Ω		8.0		ns
t _r	Rise Time			24		
t _{d(off)}	Turn-Off Delay Time			29		
t _f	Fall Time			6.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C		0.84	1.2	V
			T _J = 125°C		0.71		
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 10 A		24		ns	
t _a	Charge Time			11			
t _b	Discharge Time			12			
Q _{RR}	Reverse Recovery Charge			11			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

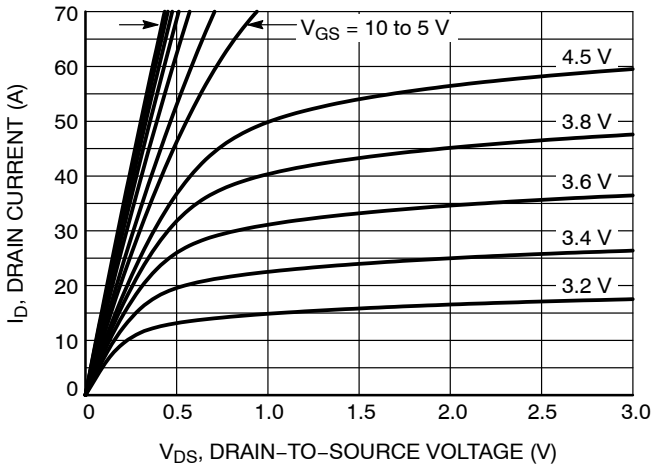


Figure 1. On-Region Characteristics

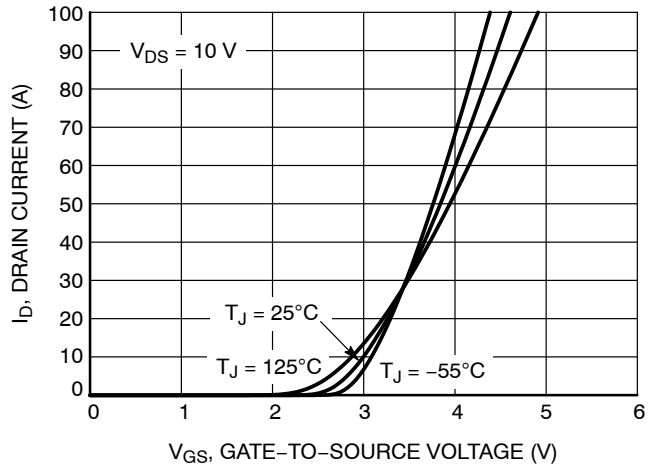


Figure 2. Transfer Characteristics

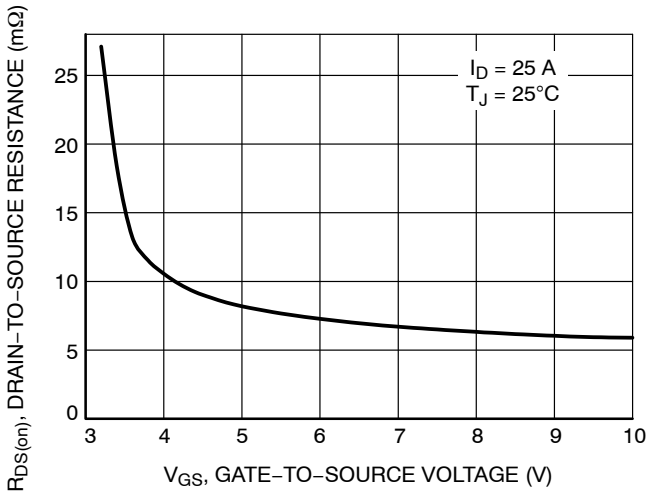


Figure 3. On-Resistance vs. Gate-to-Source Voltage

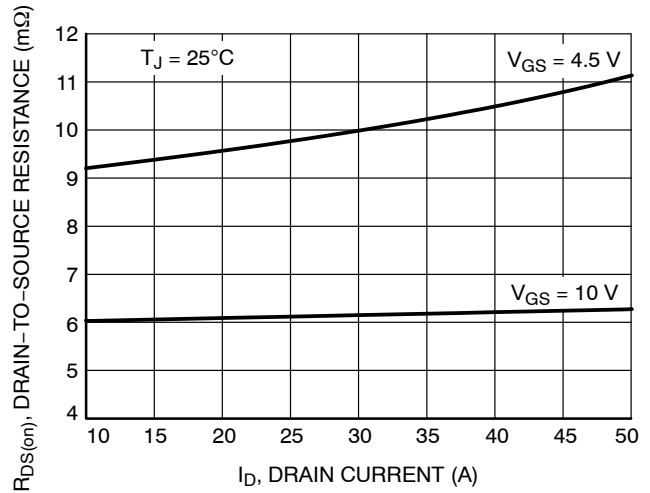


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

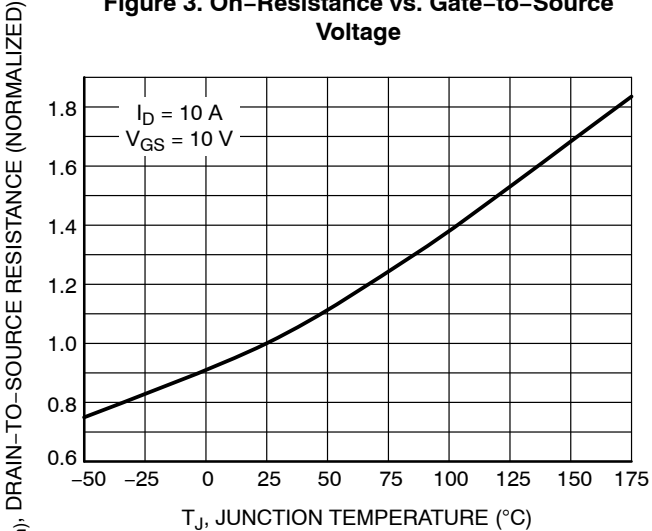


Figure 5. On-Resistance Variation with Temperature

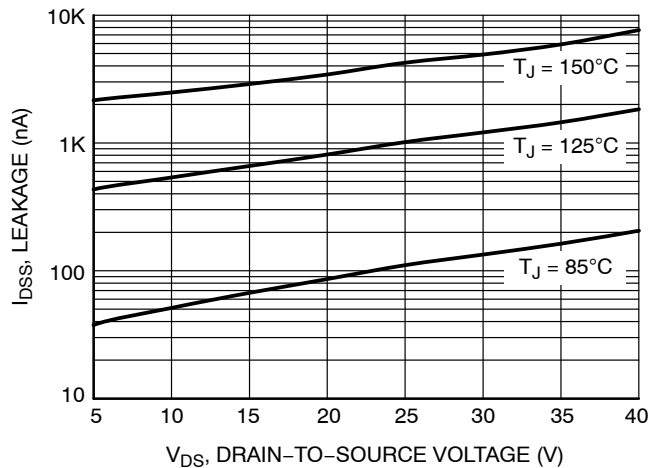


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

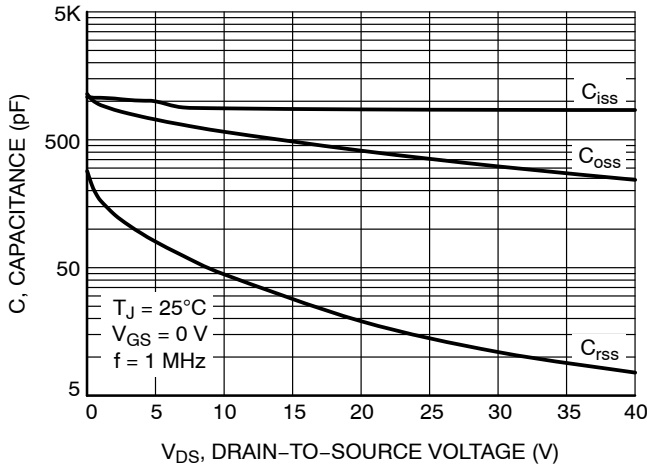


Figure 7. Capacitance Variation

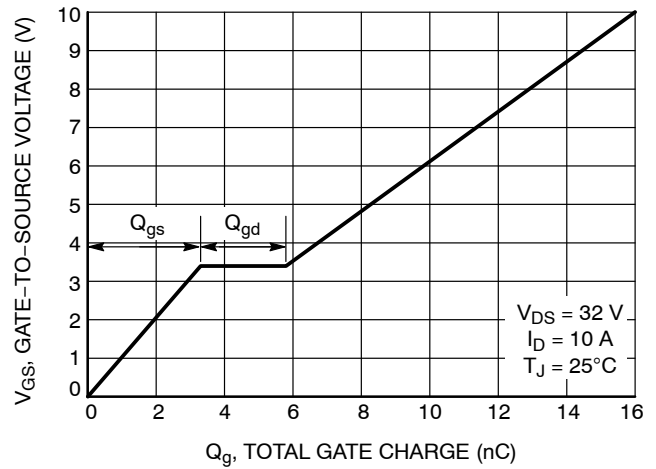


Figure 8. Gate-to-Source vs. Total Charge

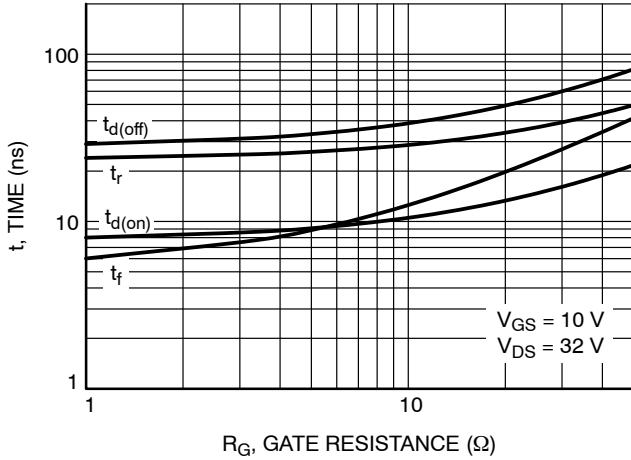


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

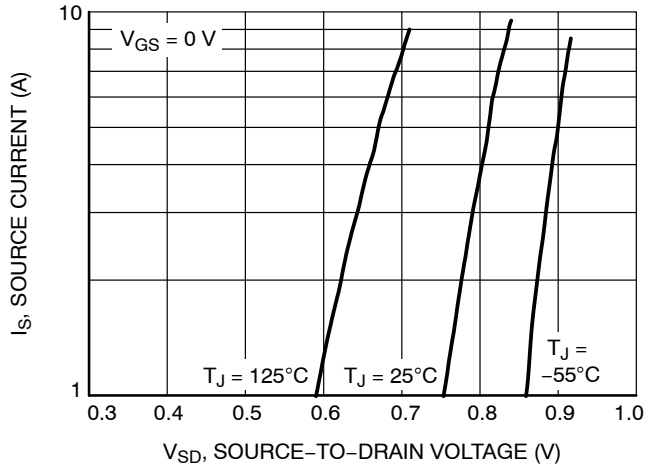


Figure 10. Diode Forward Voltage vs. Current

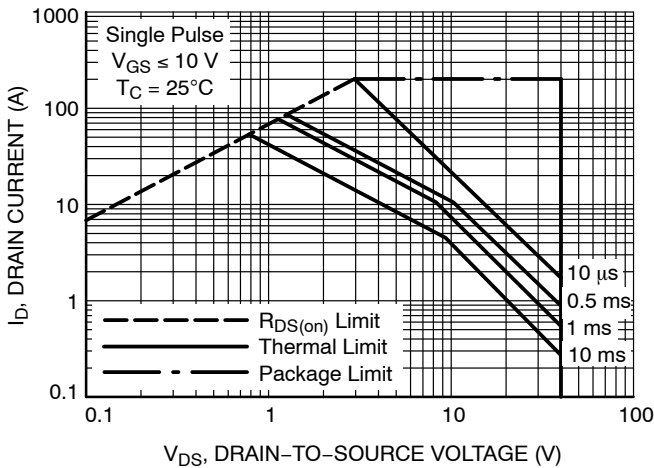


Figure 11. Maximum Rated Forward Biased Safe Operating Area

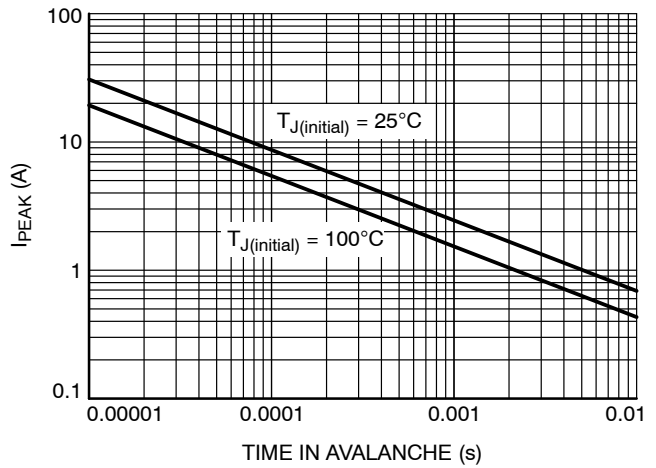


Figure 12. Maximum Drain Current vs. Time in Avalanche

NTMYS7D3N04CL

TYPICAL CHARACTERISTICS (continued)

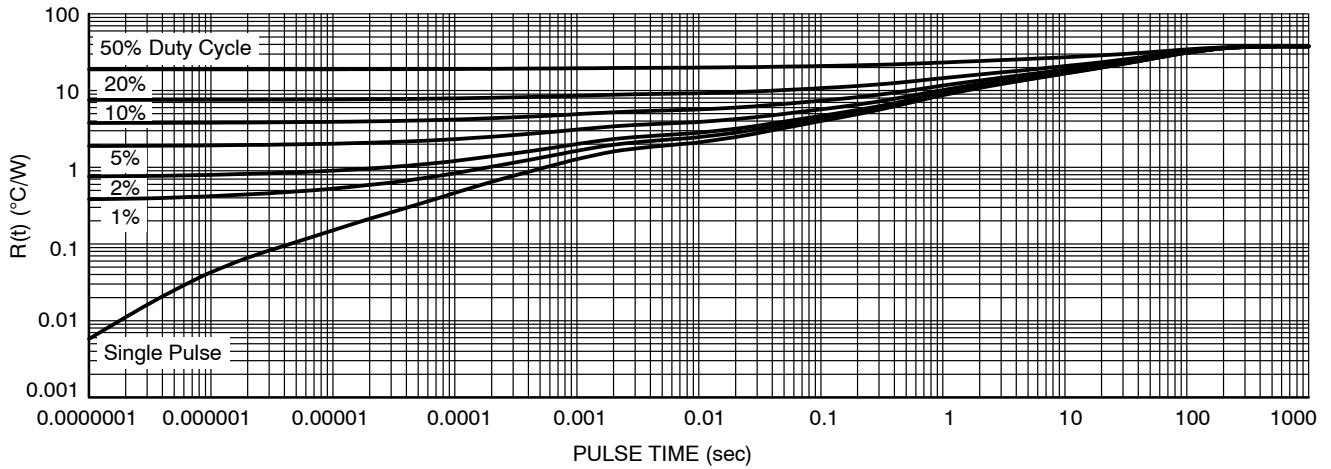


Figure 13. Thermal Characteristics

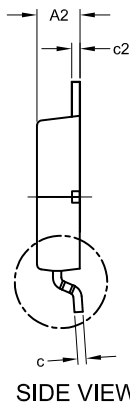
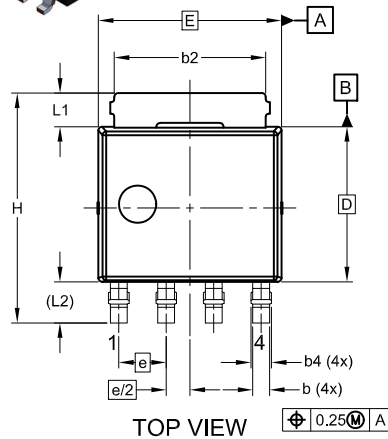
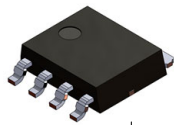
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMYS7D3N04CLTWG	7D3N04CL	LFAK4 (Pb-Free)	3,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

LFLPAK4 4.90x4.15x1.15MM, 1.27P
CASE 760AB
ISSUE D

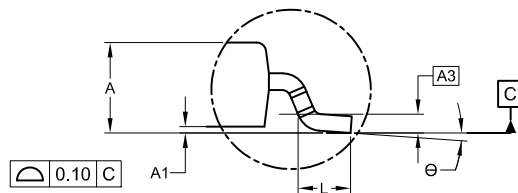
DATE 22 MAY 2024



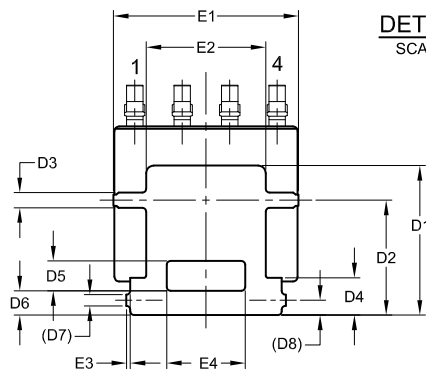
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
 4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

TOP VIEW $\text{M} \begin{matrix} \text{A} \\ 0.25 \end{matrix}$

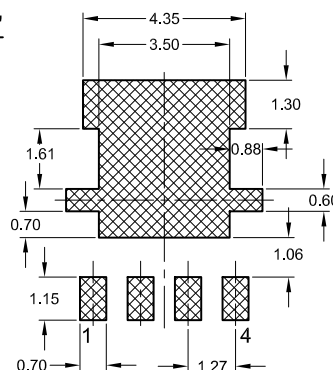
SIDE VIEW



DETAIL 'A'
SCALE: 2:1



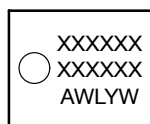
BOTTOM VIEW



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.15 BSC		
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7	0.31 REF		
D8	0.40 REF		
E	4.90 BSC		
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e	1.27 BSC		
e/2	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2	1.10 REF		
Θ	0°	4°	8°

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DESCRIPTION:	LFLPAK4 4.90x4.15x1.15MM, 1.27P	PAGE 1 OF 1

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