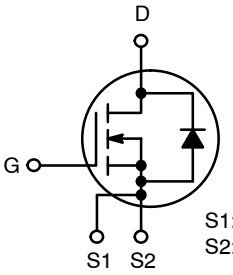
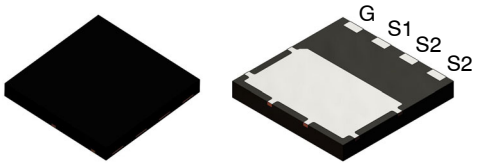
MOSFET - Power, Single N-Channel, SUPERFET® V, FRFET®, TDFN4
600 V, 61 mΩ, 41 A
NTMT061N60S5F

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
600 V	61 mΩ @ 10 V	41 A



POWER MOSFET



TDFN4 8x8 2P
CASE 520AB

Description

The SUPERFET V MOSFET FRFET series, optimized reverse recovery performance of body diode, can remove additional component and improve system reliability for soft switching applications such as PSFB and LLC. The Power88 package which is an ultra−slim SMD package offers excellent switching performance by providing kelvin source configuration and lower parasitic source inductance.

Features

- 650 V @ T_J = 150°C / Typ. $R_{DS(on)}$ = 48.8 mΩ
- 100% Avalanche Tested / MSL1 Qualified
- Kelvin Source Configuration and Low Parasitic Source Inductance
- Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Lighting / Charger/ Adapter / Industrial Power Supplies

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C, Unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	600	V
Gate−to−Source Voltage	DC	V_{GSS}	±30	V
	AC (f > 1 Hz)		±30	
Continuous Drain Current	T_C = 25°C	I_D	41	A
	T_C = 100°C		25	
Power Dissipation	T_C = 25°C	P_D	255	W
Pulsed Drain Current (Note 1)	T_C = 25°C	I_{DM}	146	A
Pulsed Source Current (Body Diode) (Note 1)	T_C = 25°C	I_{SM}	146	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)		I_S	41	A
Single Pulse Avalanche Energy	I_L = 6.7 A, R_G = 25 Ω	E_{AS}	376	mJ
Avalanche Current		I_{AS}	6.7	A
Repetitive Avalanche Energy (Note 1)		E_{AR}	2.55	mJ
MOSFET dv/dt		dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)			70	
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{SD} ≤ 20.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

MARKING DIAGRAM

NTMT061N60S5F = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTMT061N60S5F	TDFN4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case, Max.	$R_{\theta JC}$	0.49	°C/W
Thermal Resistance, Junction−to−Ambient, Max.	$R_{\theta JA}$	45	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	600	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 10 mA, Referenced to 25°C	–	630	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 600 V, T_J = 25°C	–	–	10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20.5 A, T_J = 25°C	–	48.8	61	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 4.6 mA, T_J = 25°C	3.2	–	4.8	V
Forward Trans−conductance	g_{FS}	V_{DS} = 20 V, I_D = 20.5 A	–	39	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz	–	4175	–	pF
Output Capacitance	C_{OSS}		–	63	–	
Time Related Output Capacitance	$C_{OSS(tr.)}$	I_D = Constant, V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	963	–	
Energy Related Output Capacitance	$C_{OSS(er.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	103	–	
Total Gate Charge	$Q_{G(tot)}$	V_{DD} = 400 V, I_D = 20.5 A, V_{GS} = 10 V	–	76	–	nC
Gate−to−Source Charge	Q_{GS}		–	23	–	
Gate−to−Drain Charge	Q_{GD}		–	23	–	
Gate Resistance	R_G	f = 1 MHz	–	6	–	Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 0/10 V, V_{DD} = 400 V, I_D = 20.5 A, R_G = 4.7 Ω	–	42	–	ns
Rise Time	t_r		–	15	–	
Turn−Off Delay Time	$t_{d(off)}$		–	108	–	
Fall Time	t_f		–	2.8	–	
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 20.5 A, T_J = 25°C	–	–	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_{SD} = 20.5 A, dI/dt = 100 A/μs, V_{DD} = 400 V	–	124	–	ns
Reverse Recovery Charge	Q_{RR}		–	717	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

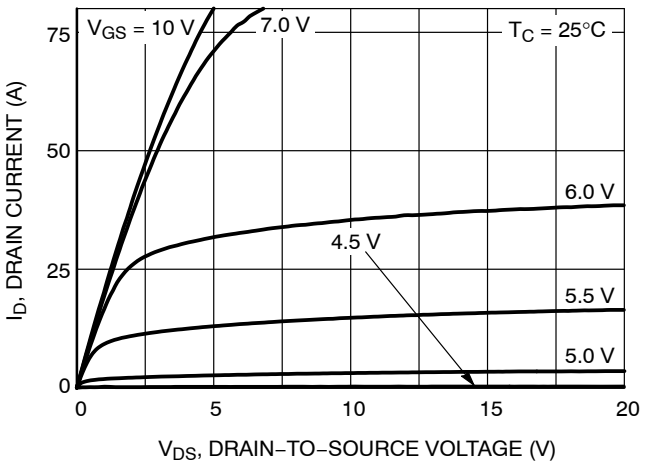


Figure 1. On−Region Characteristics

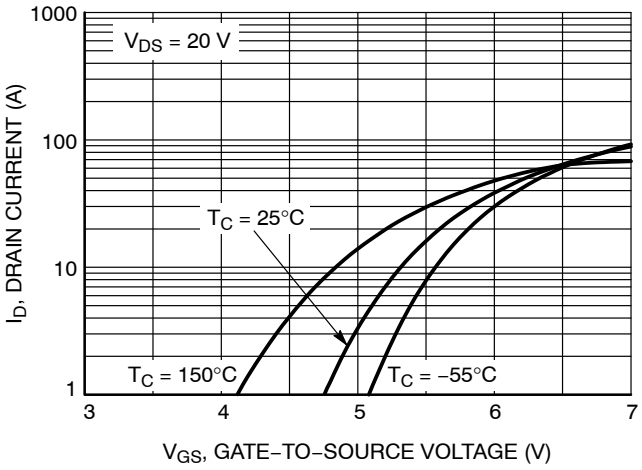


Figure 2. Transfer Characteristics

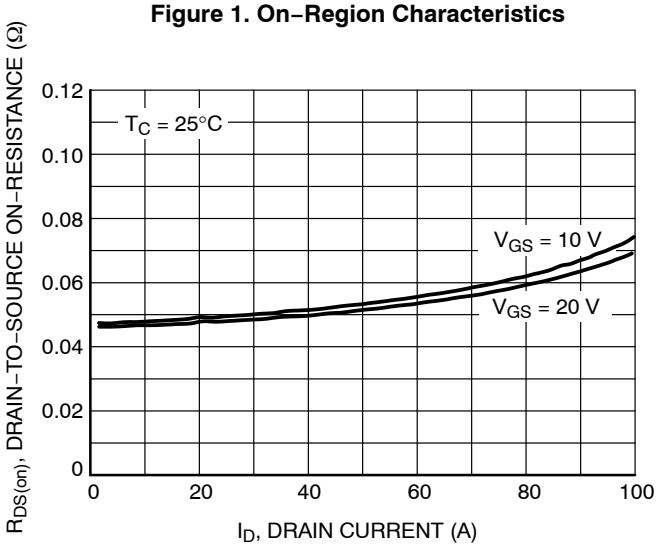


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

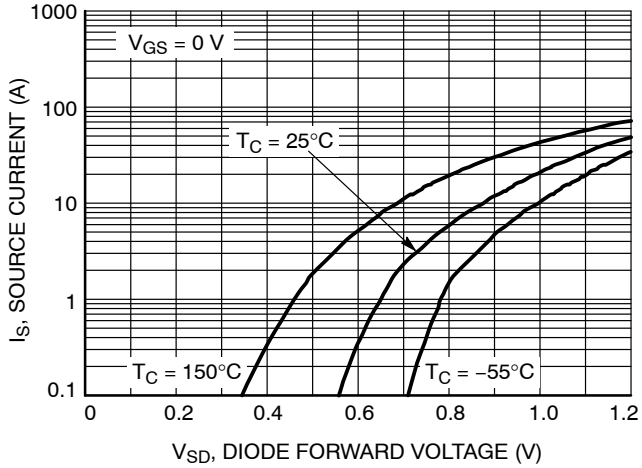


Figure 4. Diode Forward Voltage vs. Source Current

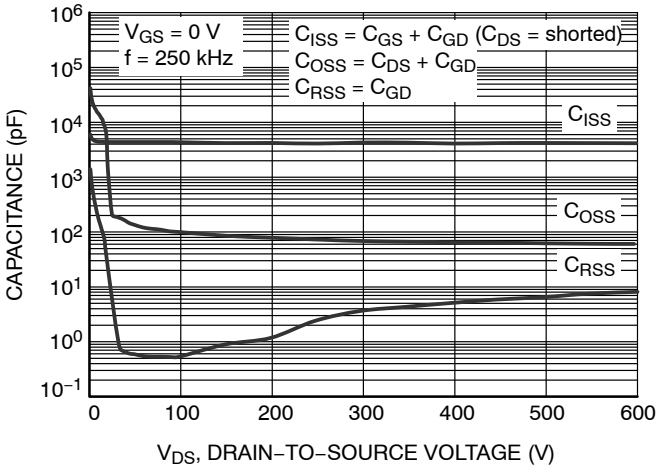


Figure 5. Capacitance Characteristics

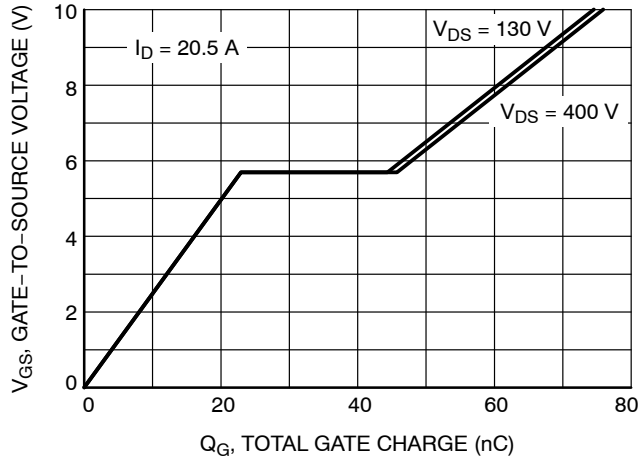


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

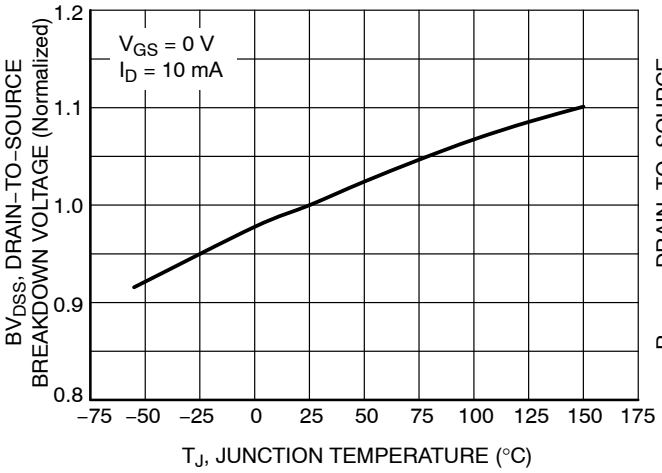


Figure 7. Breakdown Voltage Variation vs. Temperature

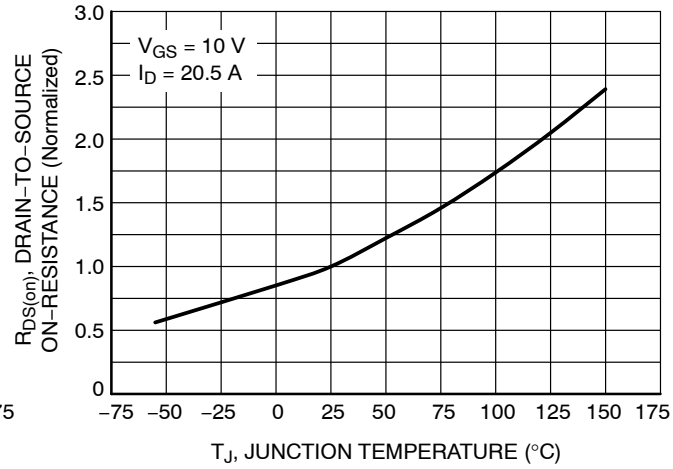


Figure 8. On−Resistance Variation vs. Temperature

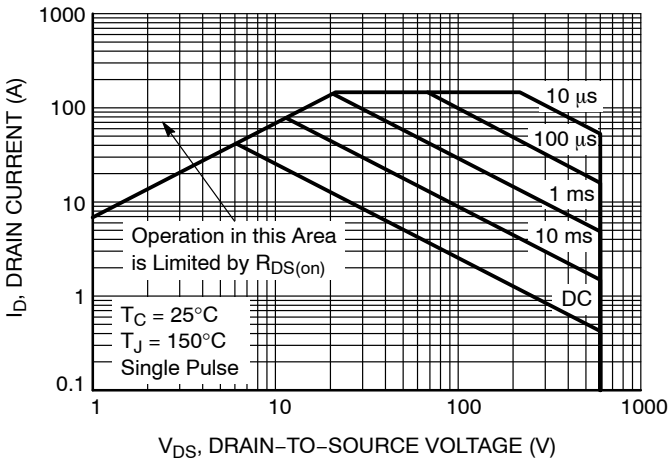


Figure 9. Maximum Safe Operating Area

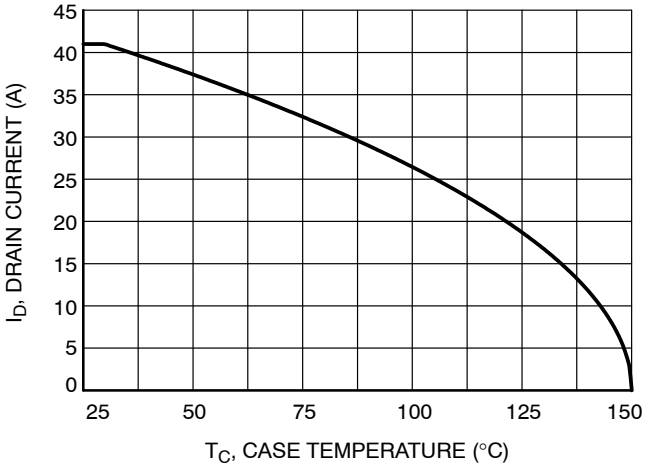


Figure 10. Maximum Drain Current vs. Case Temperature

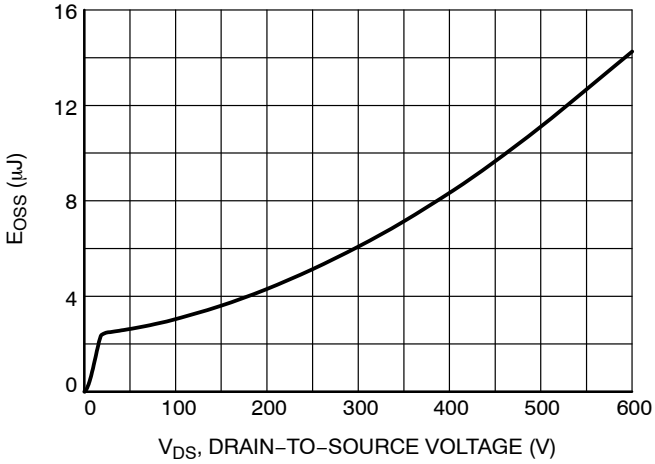


Figure 11. E_{OSS} vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

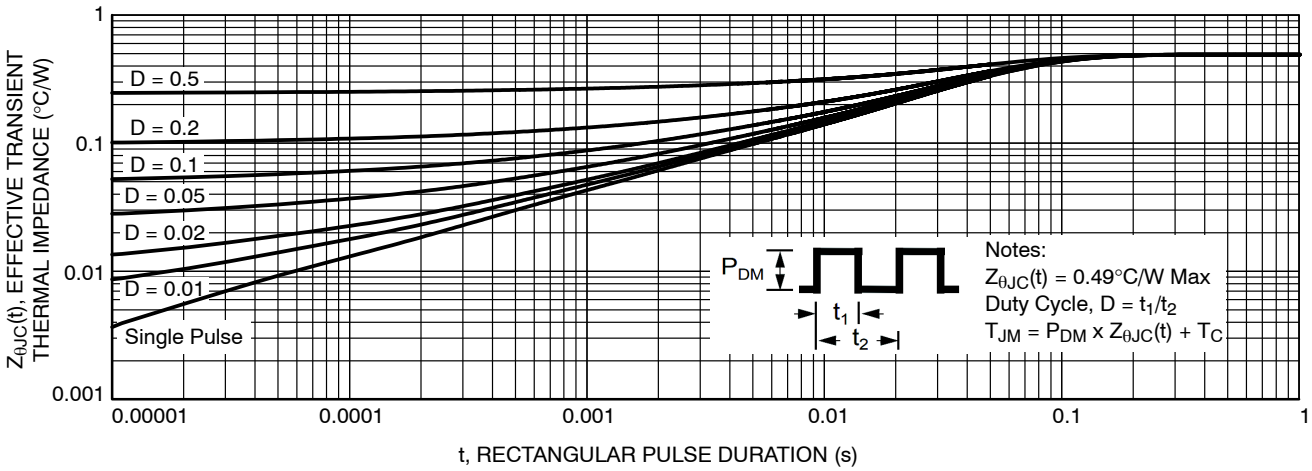


Figure 12. Transient Thermal Impedance

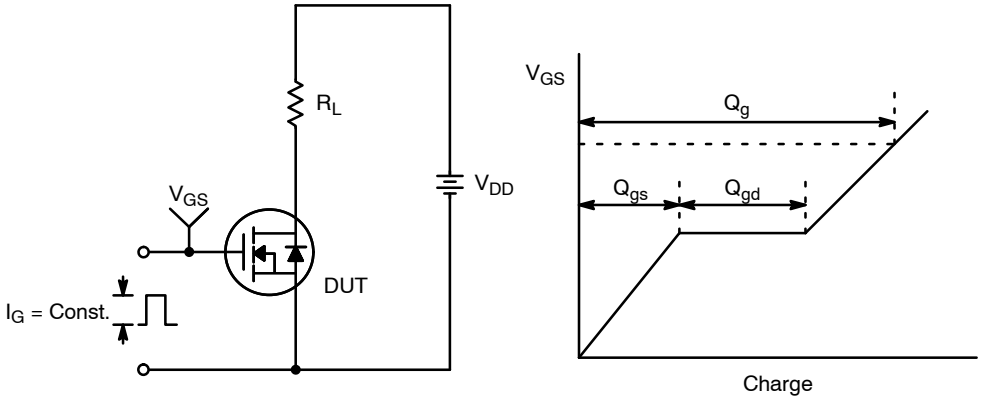


Figure 13. Gate Charge Test Circuit & Waveform

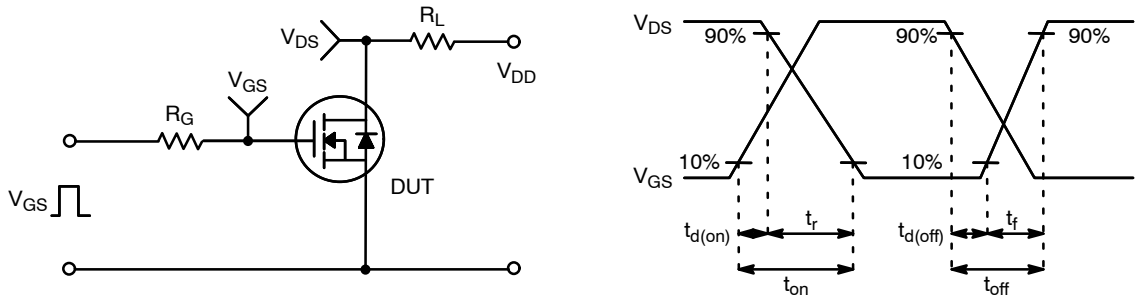


Figure 14. Resistive Switching Test Circuit & Waveforms

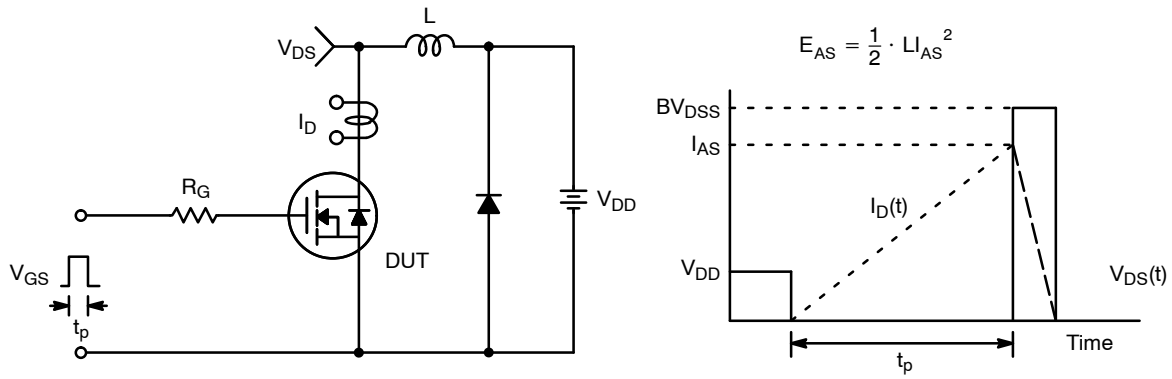


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

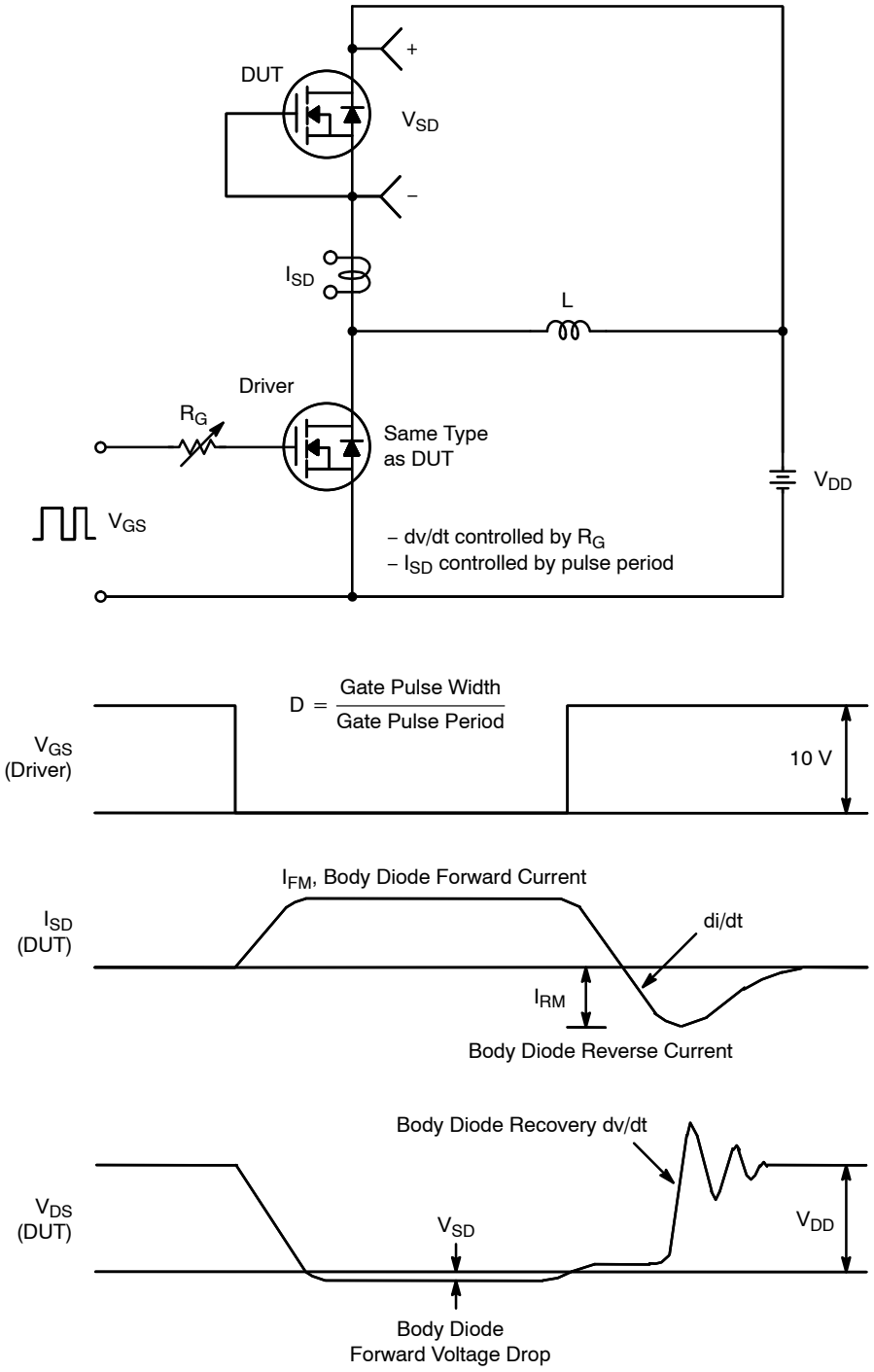
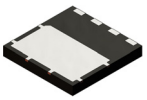


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

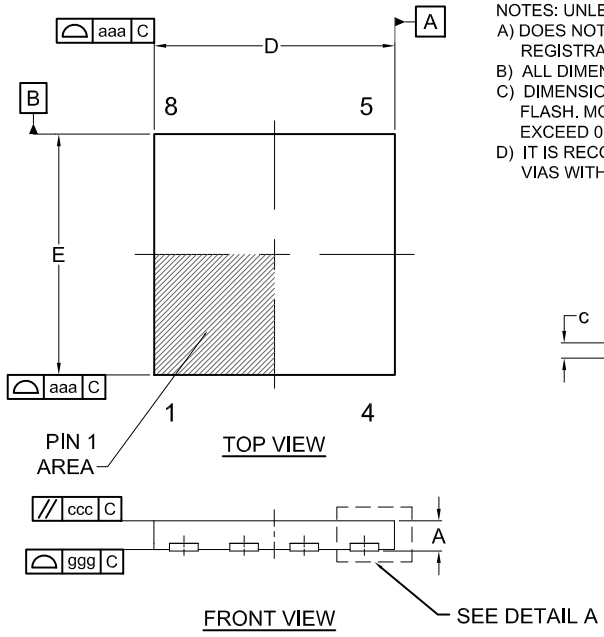
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

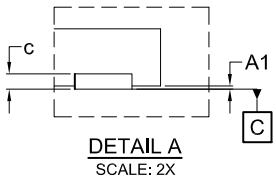


TDFN4 8x8, 2P
CASE 520AB
ISSUE O

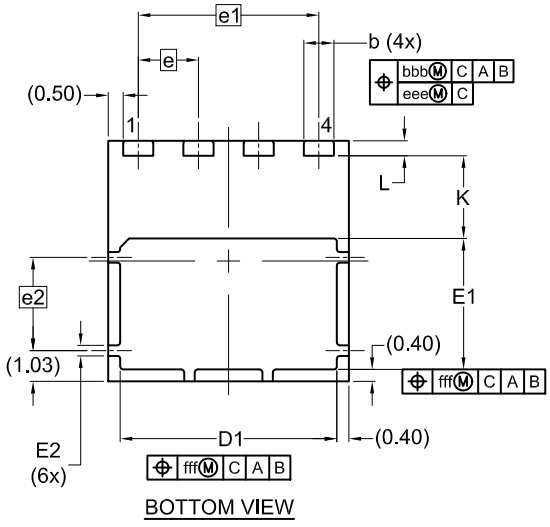
DATE 24 APR 2019

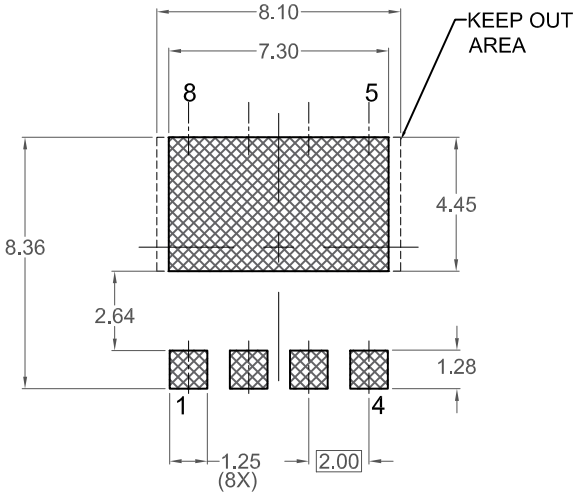


NOTES: UNLESS OTHERWISE SPECIFIED
A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
E2	0.15	0.25	0.35
e	2.00 BSC		
e1	6.00 BSC		
e2	3.10 BSC		
K	(2.75)		
L	0.40	0.50	0.60
aaa	0.10		
bbb	0.10		
ccc	0.05		
eee	0.05		
fff	0.10		
ggg	0.15		





*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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