

NTMS4N01R2

Power MOSFET

4.2 Amps, 20 Volts

N-Channel Enhancement-Mode Single SO-8 Package

Features

- High Density Power MOSFET with Ultra Low $R_{DS(on)}$ Providing Higher Efficiency
- Miniature SO-8 Surface Mount Package Saving Board Space; Mounting Information for the SO-8 Package is Provided
- I_{DSS} Specified at Elevated Temperature
- Drain-to-Source Avalanche Energy Specified
- Diode Exhibits High Speed, Soft Recovery
- Pb-Free Package is Available

Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	20	V
Drain-to-Gate Voltage ($R_{GS} = 1.0 \text{ m}\Omega$)	V_{DGR}	20	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 10	V
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.5	W
Continuous Drain Current @ 25°C	I_D	5.9	A
Continuous Drain Current @ 70°C	I_D	4.7	A
Pulsed Drain Current (Note 4)	I_{DM}	25	A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Continuous Drain Current @ 25°C	I_D	4.2	A
Continuous Drain Current @ 70°C	I_D	3.3	A
Pulsed Drain Current (Note 4)	I_{DM}	20	A
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	162	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.77	W
Continuous Drain Current @ 25°C	I_D	3.3	A
Continuous Drain Current @ 70°C	I_D	2.6	A
Pulsed Drain Current (Note 4)	I_{DM}	15	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 20 \text{ Vdc}$, $V_{GS} = 5.0 \text{ Vdc}$, Peak $I_L = 7.5 \text{ Apk}$, $L = 6 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	169	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), $t \leq 10$ seconds.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), $t =$ steady state.
3. Minimum FR-4 or G-10 PCB, $t =$ Steady State.
4. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

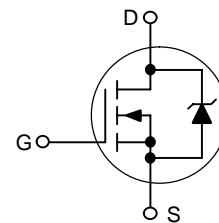


ON Semiconductor®

<http://onsemi.com>

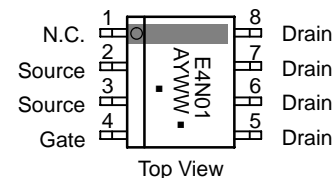
4.2 AMPERES, 20 VOLTS
0.045 Ω @ $V_{GS} = 4.5 \text{ V}$

Single N-Channel



SO-8
CASE 751
STYLE 13

MARKING DIAGRAM AND PIN ASSIGNMENT



E4N01 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4N01R2	SO-8	2500 / Tape & Reel
NTMS4N01R2G	SO-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMS4N01R2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc)	V _{(BR)DSS}	20	–	–	Vdc	
Temperature Coefficient (Positive)		–	20	–	mV/°C	
Zero Gate Voltage Drain Current (V _{DS} = 12 Vdc, V _{GS} = 0 Vdc, T _J = 25°C) (V _{DS} = 12 Vdc, V _{GS} = 0 Vdc, T _J = 125°C) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 25°C)	I _{DSS}	–	–	1.0	μAdc	
		–	–	10		
		–	0.2	–		
Gate-Body Leakage Current (V _{GS} = +10 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	100	nAdc	
Gate-Body Leakage Current (V _{GS} = -10 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	-100	nAdc	
ON CHARACTERISTICS						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc)	V _{GS(th)}	0.6	0.95	1.2	Vdc	
Temperature Coefficient (Negative)		–	-3.0	–	mV/°C	
Static Drain-to-Source On-State Resistance (V _{GS} = 4.5 Vdc, I _D = 4.2 Adc) (V _{GS} = 2.7 Vdc, I _D = 2.1 Adc) (V _{GS} = 2.5 Vdc, I _D = 2.0 Adc)	R _{DS(on)}	–	0.030	0.04	Ω	
		–	0.035	0.05		
		–	0.037	–		
Forward Transconductance (V _{DS} = 2.5 Vdc, I _D = 2.0 Adc)	g _{FS}	–	10	–	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V _{DS} = 10 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{ISS}	–	870	1200	pF
Output Capacitance		C _{OSS}	–	260	400	
Reverse Transfer Capacitance		C _{RSS}	–	60	100	
SWITCHING CHARACTERISTICS (Notes 6 & 7)						
Turn-On Delay Time	(V _{DD} = 12 Vdc, I _D = 4.2 Adc, V _{GS} = 4.5 Vdc, R _G = 2.3 Ω)	t _{d(on)}	–	13	25	ns
Rise Time		t _r	–	35	65	
Turn-Off Delay Time		t _{d(off)}	–	45	75	
Fall Time		t _f	–	50	90	
Total Gate Charge	(V _{DS} = 12 Vdc, V _{GS} = 4.5 Vdc, I _D = 4.2 Adc)	Q _{tot}	–	11	16	nC
Gate-Source Charge		Q _{gs}	–	2.0	–	
Gate-Drain Charge		Q _{gd}	–	3.0	–	
BODY-DRAIN DIODE RATINGS (Note 6)						
Diode Forward On-Voltage (I _S = 4.2 Adc, V _{GS} = 0 Vdc) (I _S = 4.2 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	–	0.85	1.1	Vdc	
		–	0.70	–		
Reverse Recovery Time	(I _S = 4.2 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs)	t _{rr}	–	20	–	ns
		t _a	–	12	–	
		t _b	–	8.0	–	
Reverse Recovery Stored Charge	Q _{RR}	–	0.01	–	μC	

5. Handling precautions to protect against electrostatic discharge is mandatory.

6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

7. Switching characteristics are independent of operating junction temperature.

NTMS4N01R2

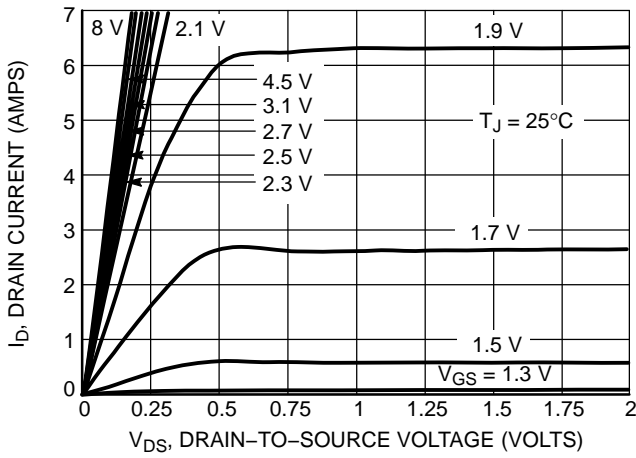


Figure 1. On-Region Characteristics

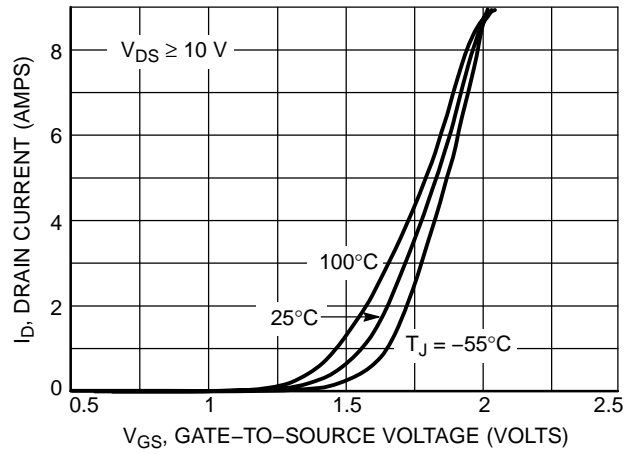


Figure 2. Transfer Characteristics

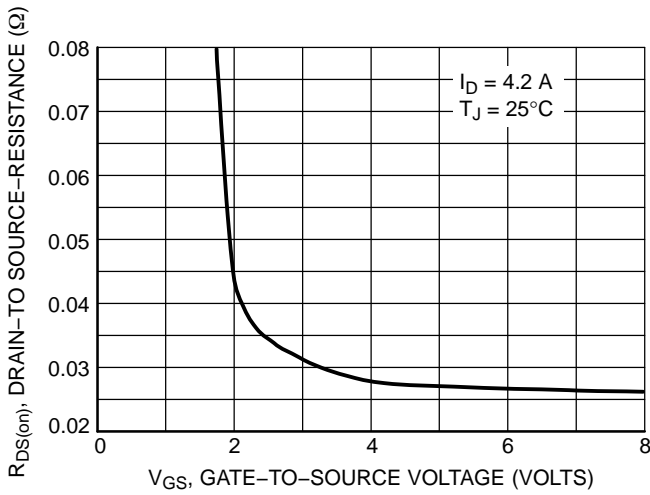


Figure 3. On-Resistance versus Gate-to-Source Voltage

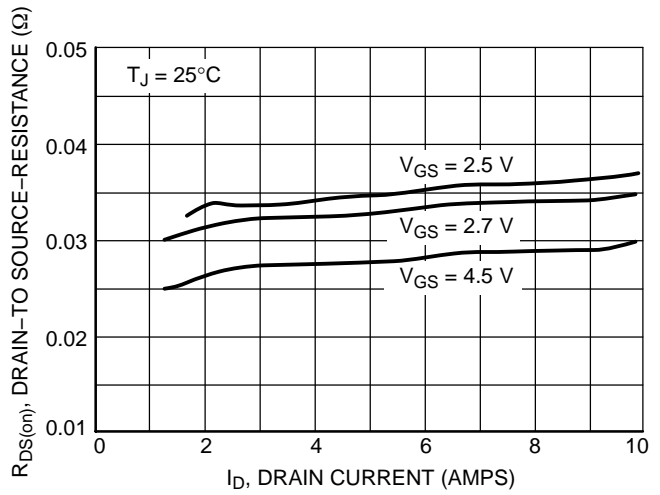


Figure 4. On-Resistance versus Drain Current and Gate Voltage

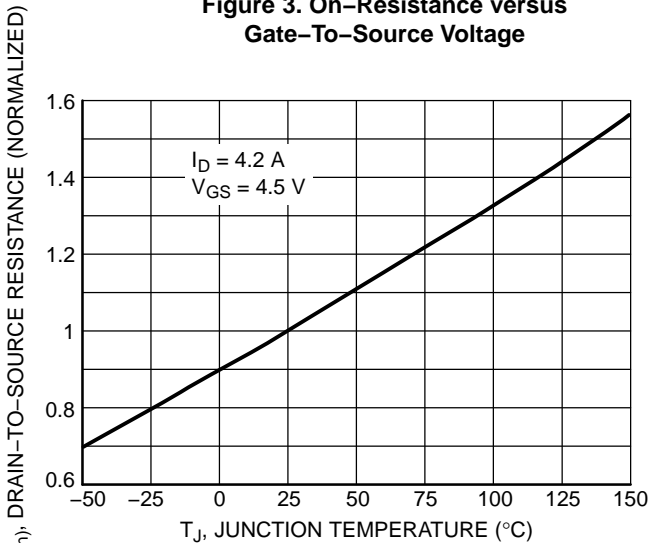


Figure 5. On-Resistance Variation with Temperature

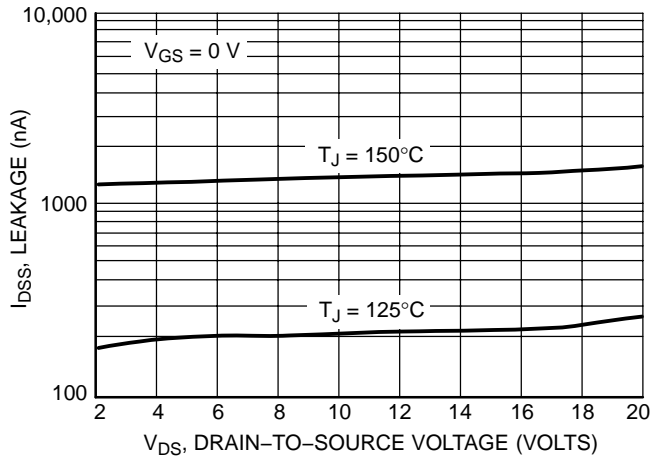


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTMS4N01R2

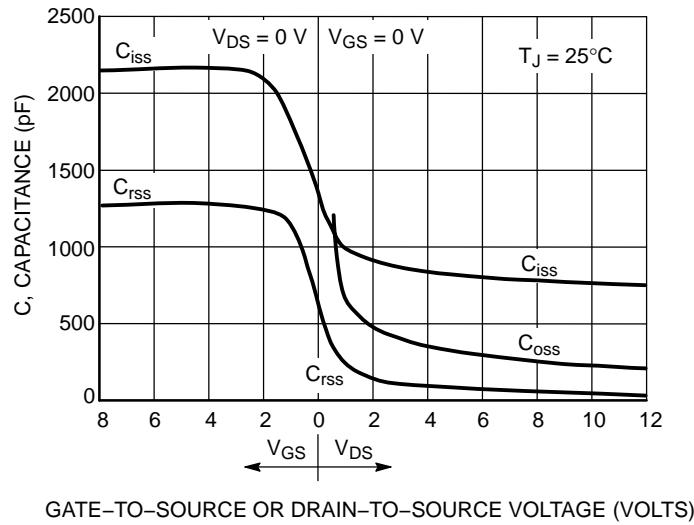


Figure 7. Capacitance Variation

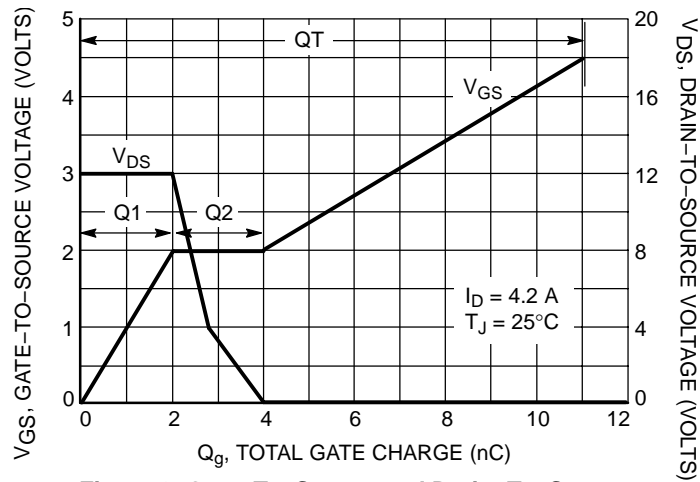


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

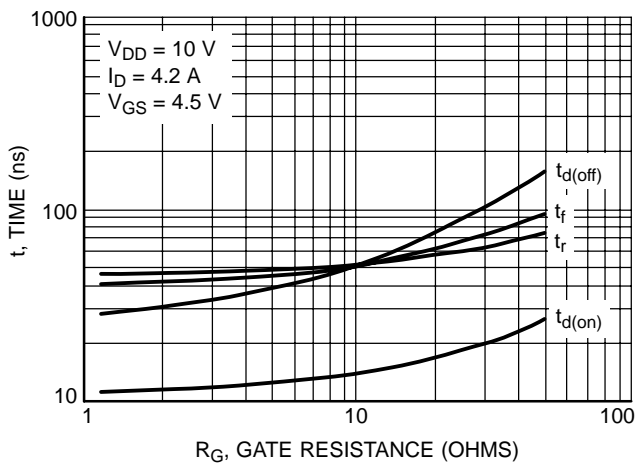


Figure 9. Resistive Switching Time Variation versus Gate Resistance

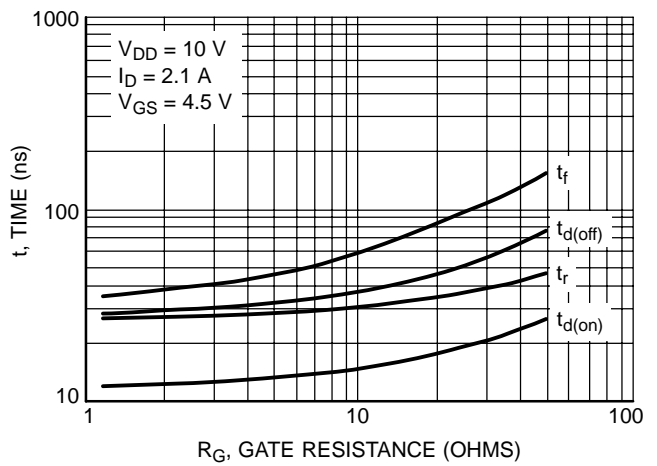


Figure 10. Resistive Switching Time Variation versus Gate Resistance

NTMS4N01R2

DRAIN-TO-SOURCE DIODE CHARACTERISTICS

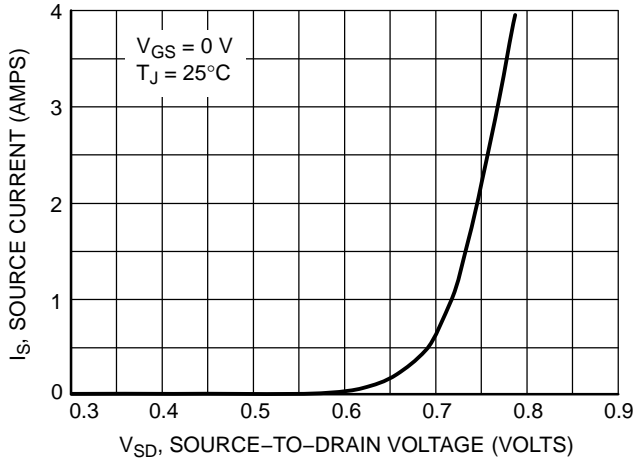


Figure 11. Diode Forward Voltage versus Current

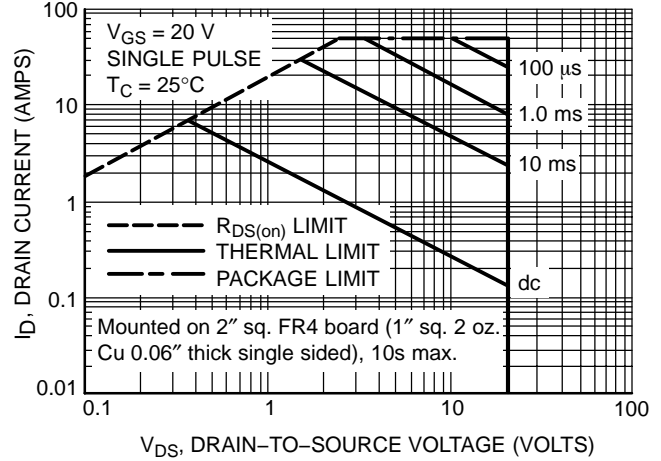


Figure 12. Maximum Rated Forward Biased Safe Operating Area

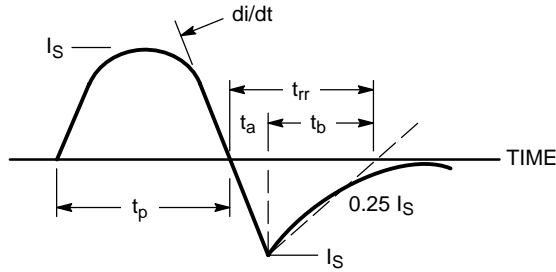


Figure 13. Diode Reverse Recovery Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

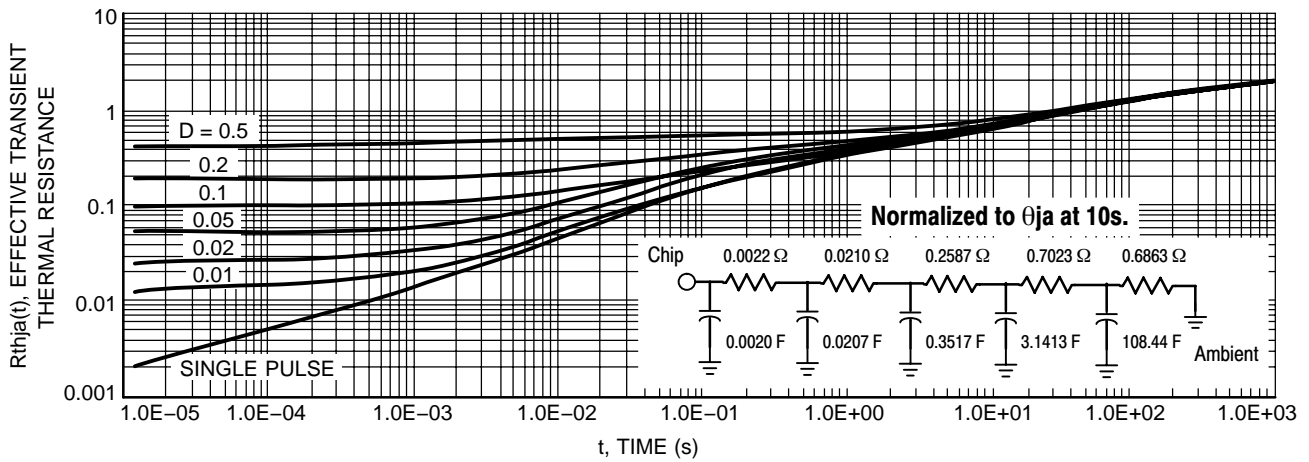


Figure 14. Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales