

MOSFET - Power, Single N-Channel, LPAK8

30 V, 0.65 mΩ, 410 A

NTMJS0D7N03CG

Features

- Wide SOA to Improve Inrush Current Management
- Advanced LPAK Package (5x6mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- These Devices are Pb-Free, Halogen/BFR-Free and are RoHS Compliant

Typical Applications

- Hot Swap Application
- Motor Drive
- Power Load Switch
- Battery Management

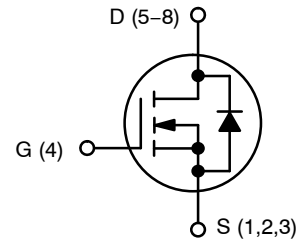
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit |
|--|--|---------------------------|------------------|
| Drain-to-Source Voltage | V_{DSS} | 30 | V |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | Steady State | $T_C = 25^\circ\text{C}$ | I_D 410 A |
| | | $T_C = 100^\circ\text{C}$ | 290 |
| | | $T_C = 25^\circ\text{C}$ | P_D 188 W |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 59 A |
| | | $T_A = 100^\circ\text{C}$ | 42 |
| | | $T_A = 25^\circ\text{C}$ | P_D 4.0 W |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 900 | A |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 40.8 \text{ A}$) | E_{AS} | 1080 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

| $V_{(BR)DSS}$ | $R_{DS(ON) MAX}$ | $I_D MAX$ |
|---------------|------------------|-----------|
| 30 V | 0.65 mΩ @ 10 V | 410 A |

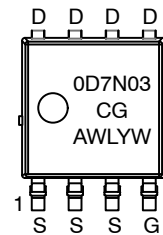


N-CHANNEL MOSFET



LPAK8 CASE 760AA

MARKING DIAGRAM



0D7N03CG = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NTMJS0D7N03CG

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Junction-to-Case – Steady State (Note 1) | $R_{\theta JC}$ | 0.8 | °C/W |
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 38 | |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 134 | |

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|-------------------|--|---------------------------|----|-----|---------------|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 30 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D = 250\ \mu\text{A}$, ref to 25°C | | 11 | | mV/°C |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 1.0 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 100 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|-----------------------------------|------------------|--|-----|------|------|------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 280\ \mu\text{A}$ | 1.3 | | 2.2 | V |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D = 280\ \mu\text{A}$, ref to 25°C | | -5.1 | | mV/°C |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 30\text{ A}$ | | 0.55 | 0.65 | m Ω |
| Forward Transconductance | g_{FS} | $V_{DS} = 3\text{ V}, I_D = 30\text{ A}$ | | 100 | | S |
| Gate Resistance | R_G | $T_A = 25^\circ\text{C}$ | | 0.4 | | Ω |

CHARGES & CAPACITANCES

| | | | | | | |
|------------------------------|--------------|---|--|-------|--|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$ | | 12300 | | pF |
| Output Capacitance | C_{OSS} | | | 5800 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 88 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$ | | 147 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 19 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 8.6 | | |
| Gate-to-Source Charge | Q_{GS} | | | 34 | | |

SWITCHING CHARACTERISTICS (Note 4)

| | | | | | | |
|---------------------|--------------|--|--|----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}, R_G = 3\ \Omega$ | | 28 | | ns |
| Rise Time | t_r | | | 13 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 85 | | |
| Fall Time | t_f | | | 16 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|---|---------------------------|--|------|-----|----|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 30\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.78 | 1.2 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.62 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, V_R = 15\text{ V}, I_S = 30\text{ A}, dI_S/dt = 100\text{ A}/\mu\text{s}$ | | | 98 | | ns |
| Reverse Recovery Charge | Q_{RR} | | | | 143 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

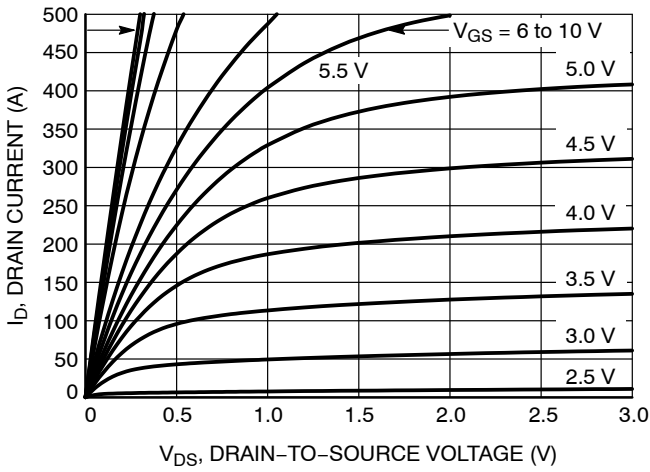


Figure 1. On-Region Characteristics

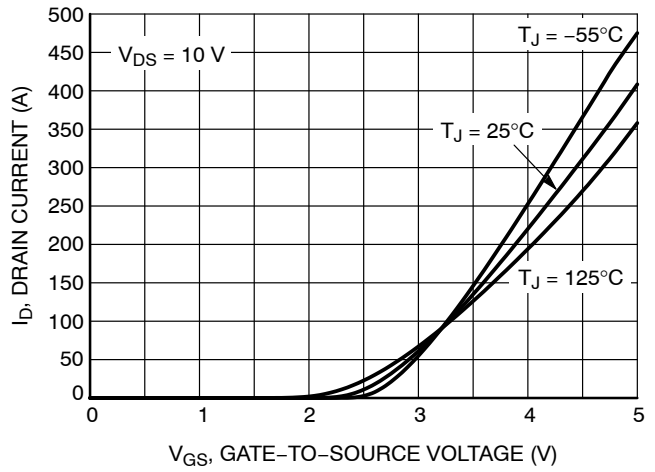


Figure 2. Transfer Characteristics

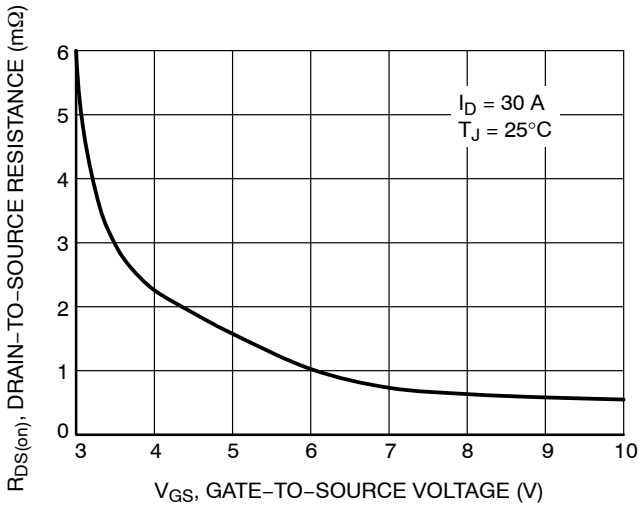


Figure 3. On-Resistance vs. Gate-to-Source Voltage

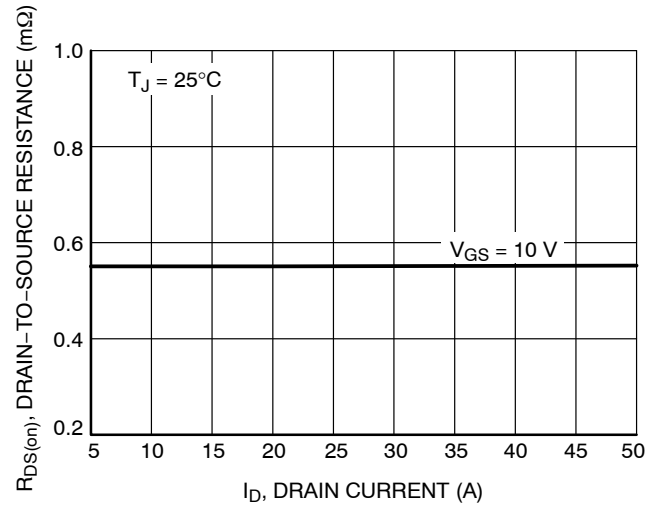


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

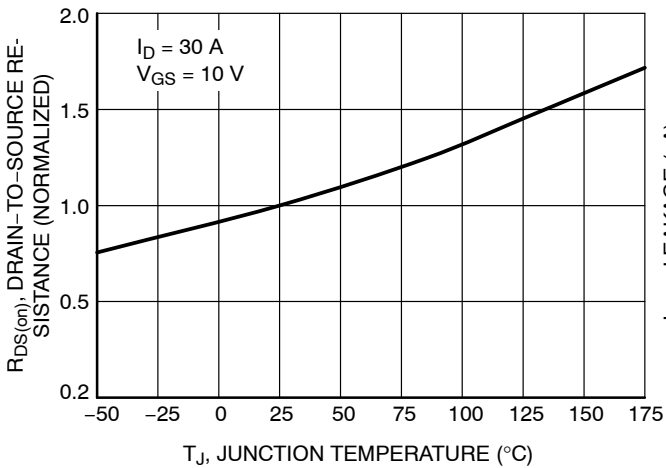


Figure 5. On-Resistance Variation with Temperature

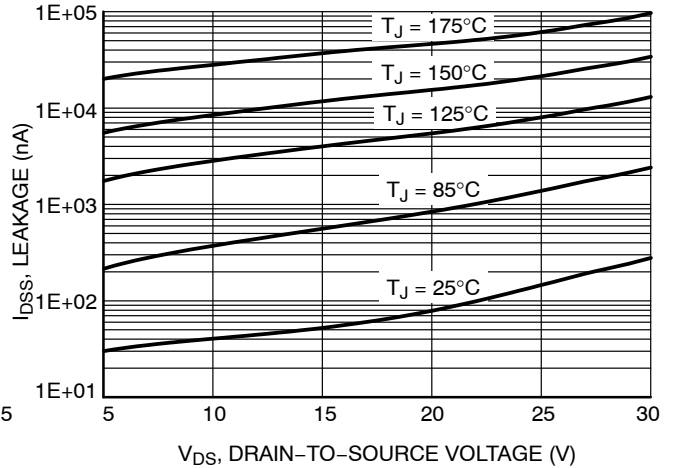


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

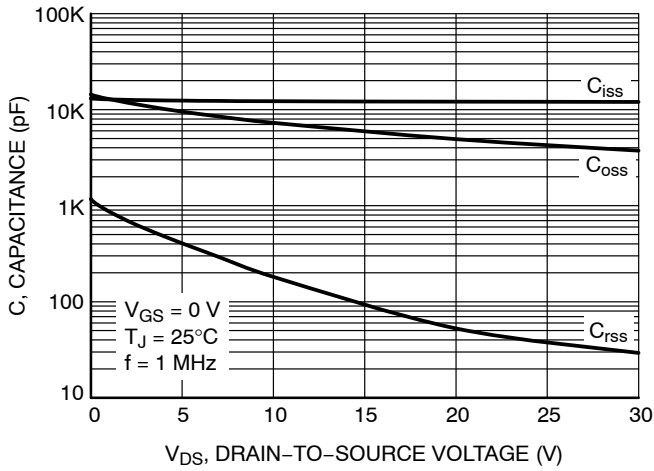


Figure 7. Capacitance Variation

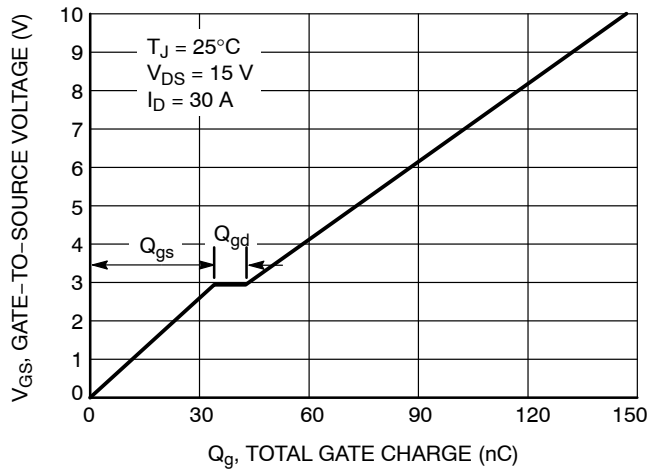


Figure 8. Gate-to-Source vs. Total Charge

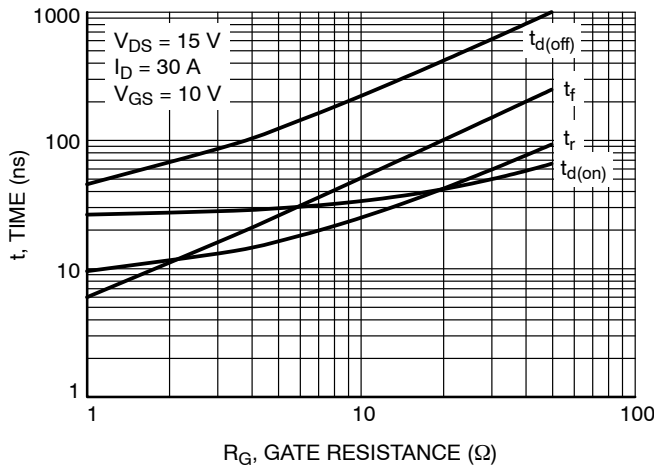


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

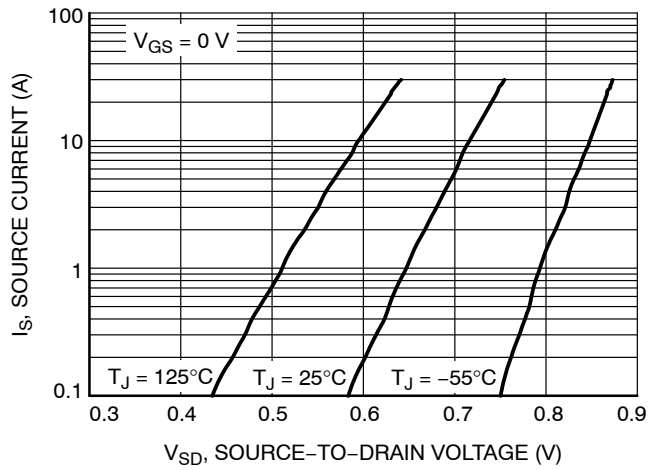


Figure 10. Diode Forward Voltage vs. Current

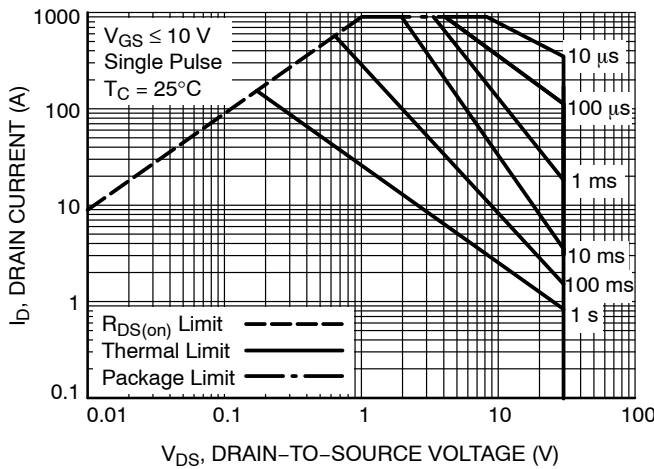


Figure 11. Maximum Rated Forward Biased Safe Operating Area

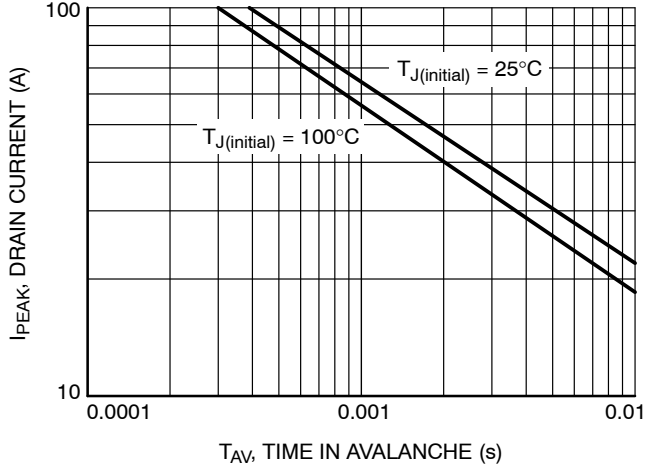


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

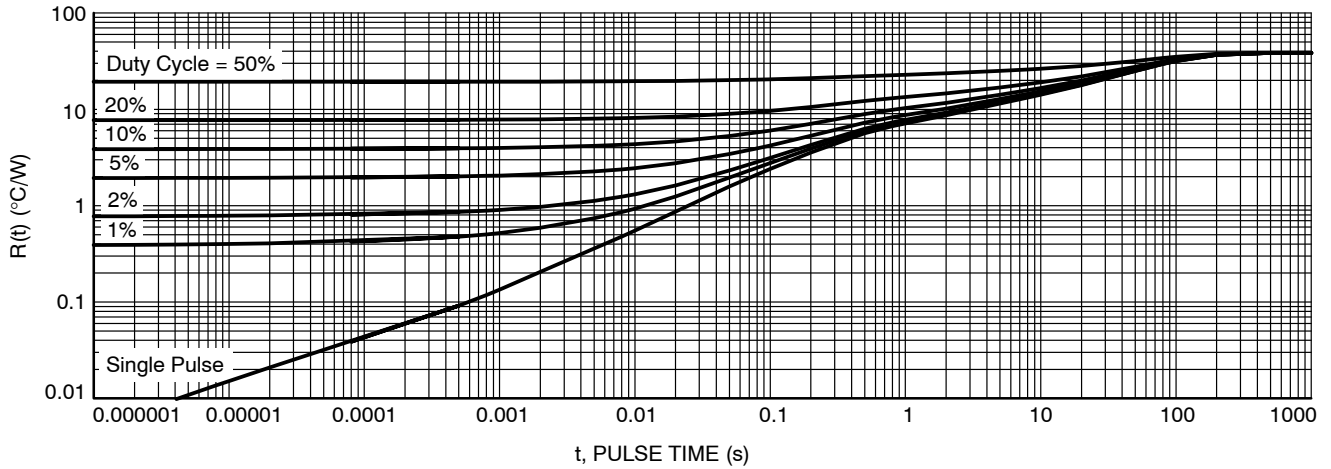


Figure 13. Thermal Response

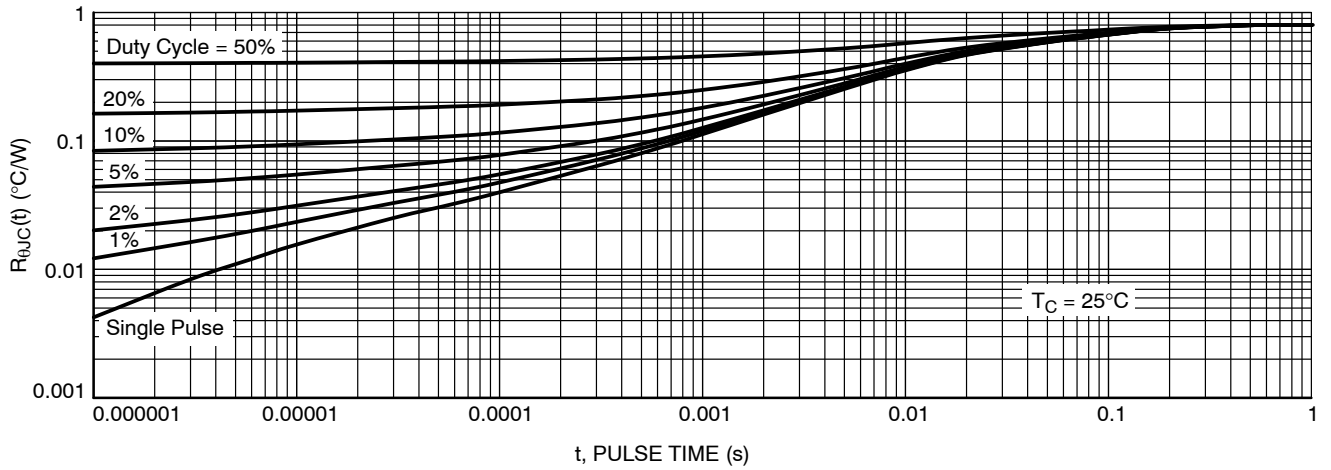


Figure 14. Thermal Response

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|------------------|--------------|---------------------|--------------------|
| NTMJS0D7N03CGTWG | 0D7N03 CG | LFPAK8 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

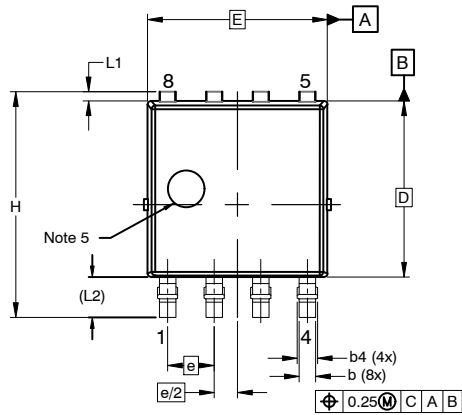
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



LPAK8 4.90x4.80x1.12MM, 1.27P
CASE 760AA
ISSUE D

DATE 22 APR 2024



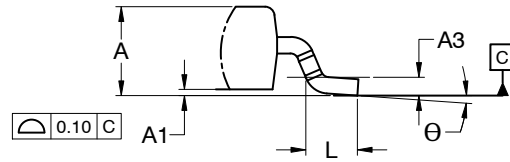
TOP VIEW



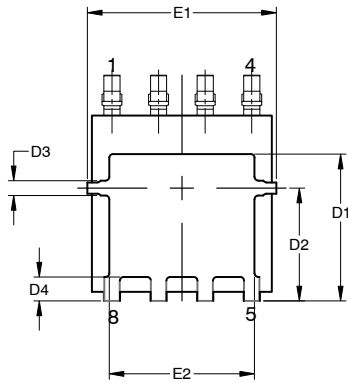
SIDE VIEW

NOTES:

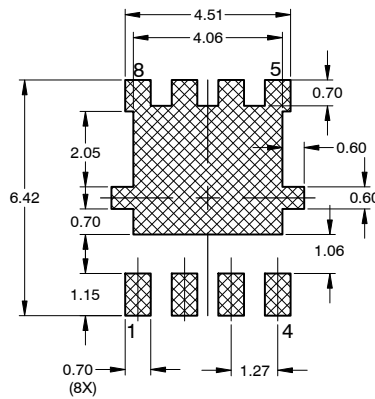
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.



DETAIL 'A'



BOTTOM VIEW

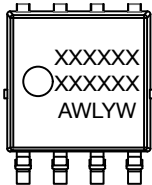


RECOMMENDED LAND PAD

| MILLIMETERS | | | |
|-------------|-----------|------|------|
| DIM | MIN | NOM | MAX |
| A | 1.10 | 1.20 | 1.30 |
| A1 | 0.00 | 0.08 | 0.15 |
| A2 | 1.10 | 1.15 | 1.20 |
| A3 | 0.25 BSC | | |
| b | 0.40 | 0.45 | 0.50 |
| b4 | 0.45 | 0.55 | 0.65 |
| c | 0.19 | 0.22 | 0.25 |
| c2 | 0.19 | 0.22 | 0.25 |
| D | 4.70 | 4.80 | 4.90 |
| D1 | 3.80 | 4.00 | 4.20 |
| D2 | 2.98 | 3.08 | 3.18 |
| D3 | 0.30 | 0.40 | 0.50 |
| D4 | 0.55 | 0.65 | 0.75 |
| E | 4.80 | 4.90 | 5.00 |
| E1 | 5.05 | 5.15 | 5.25 |
| E2 | 3.91 | 3.96 | 4.01 |
| e | 1.27 BSC | | |
| e/2 | 0.635 BSC | | |
| H | 6.00 | 6.15 | 6.30 |
| L | 0.50 | 0.70 | 0.90 |
| L1 | 0.15 | 0.25 | 0.35 |
| L2 | 1.10 REF | | |
| θ | 0° | 4° | 8° |

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

| | | |
|-------------------------|--------------------------------------|--|
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| DESCRIPTION: | LPAK8 4.90x4.80x1.12MM, 1.27P | PAGE 1 OF 1 |

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