

MOSFET - Power, Single N-Channel, DUAL COOL[®]

80 V, 10 mΩ, 61 A

NTMFSC010N08M7

Features

- DUAL COOL Top Side Cooling PQFN Package
- Max $r_{DS(on)}$ = 10 mΩ at $V_{GS} = 10$ V, $I_D = 10$ A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

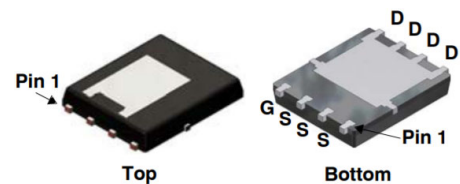
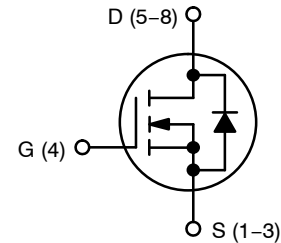
Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	80	V	
Gate-to-Source Voltage	V_{GS}	±20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D 61	A
		$T_C = 100^\circ\text{C}$	38.6	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D 78.1	W
		$T_C = 100^\circ\text{C}$	31.2	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D 12.5	A
		$T_A = 100^\circ\text{C}$	7.9	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D 3.3	W
		$T_A = 100^\circ\text{C}$	1.3	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM} 180	A	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	61	A	
Single Pulse Drain-to-Source Avalanche Energy ($L_{L(pk)} = 3.9$ A)	E_{AS}	640	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

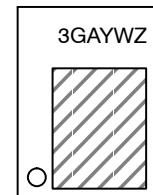
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	10 mΩ @ 10 V	61 A

N-Channel MOSFET



DFN8 5x6
(Dual Cool 56)
CASE 506EG

MARKING DIAGRAM



- 3G = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping
NTMFSC010N08M7	DFN8 (Pb-Free)	3000 / Tape & Reel

NTMFSC010N08M7

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain to Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			49		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V T _J = 25°C			1	μA
Zero Gate Voltage Drain Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			±100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 120 μA	2.5	3.3	4.5	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-9		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V I _D = 10 A		7.6	10	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 5 V I _D = 10 A		21.5	40	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1 MHz	V _{DS} = 0 V		2373		pF
	C _{iss}		V _{DS} = 40 V		2080	2700	
Output Capacitance	C _{oss}				286	430	
Reverse Transfer Capacitance	C _{rss}				11	17	
Gate Resistance	R _g	V _{GS} = 0.5 V, f = 1MHz			1	2.6	Ω
Threshold Gate Charge	Q _{g(th)}	V _{GS} = 0 to 2 V	V _{GS} = 10 V, V _{DS} = 40 V; I _D = 10 A		4.3		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 0 to 10 V			29.3	38	
Gate to Source Gate Charge	Q _{gs}	V _{GS} = 0 to 10 V			11.8		
Gate to Drain "Miller" Charge	Q _{gd}				4.3		
Plateau Voltage	V _{GP}				5.5		V
Output Charge	Q _{oss}	V _{DS} = 40 V, V _{GS} = 0 V			26		nC

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{DD} = 40 V, I _D = 10 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		14		ns
Turn-On Rise Time	t _r			6		ns
Turn-Off Delay Time	t _{d(OFF)}			27		ns
Turn-Off Fall Time	t _f			6		ns

DRAIN – SOURCE DIODE CHARACTERISTICS

Source to Drain Diode Voltage	V _{SD}	I _{SD} = 10 A, V _{GS} = 0 V		0.82	1.2	V
Reverse Recovery Time	T _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs, I _S = 10 A		41	50	ns
Charge Time	t _a			24.6		
Discharge Time	t _b			16.1		
Reverse Recovery Charge	Q _{RR}			45	58	nC

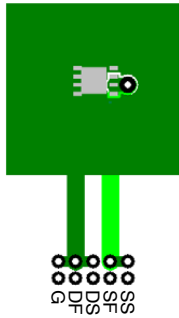
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case (Top Source)	1.6	°C/W
R _{θJC}	Thermal Resistance, Junction to Case (Bottom Drain)	3.0	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	38	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1b)	81	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1c)	27	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1d)	34	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1e)	16	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1f)	19	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1g)	26	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1h)	61	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1i)	16	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1j)	23	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1k)	11	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1l)	13	

6. R_{θJA} is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. R_{θJA} is guaranteed by design while R_{CA} is determined by the user's board design.



a) 38°C/W when mounted on a 1 in2 pad of 2 oz copper.



b) 81°C/W when mounted on a minimum pad of 2 oz copper.

- c) Still air, 20.9-10.4-12.7 mm Aluminum Heat Sink, 1 in2 pad of 2 oz copper
- d) Still air, 20.9-10.4-12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e) Still air, 45.2-41.4-11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in2 pad of 2 oz copper
- f) Still air, 45.2-41.4-11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g) .200FPM Airflow, No Heat Sink, 1 in2 pad of 2 oz copper
- h) .200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i) .200FPM Airflow, 20.9-10.4-12.7 mm Aluminum Heat Sink, 1 in2 pad of 2 oz copper
- j) .200FPM Airflow, 20.9-10.4-12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k) .200FPM Airflow, 45.2-41.4-11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in2 pad of 2 oz copper
- l) .200FPM Airflow, 45.2-41.4-11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

7. Pulse Test: Pulse Width < 300 _s, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

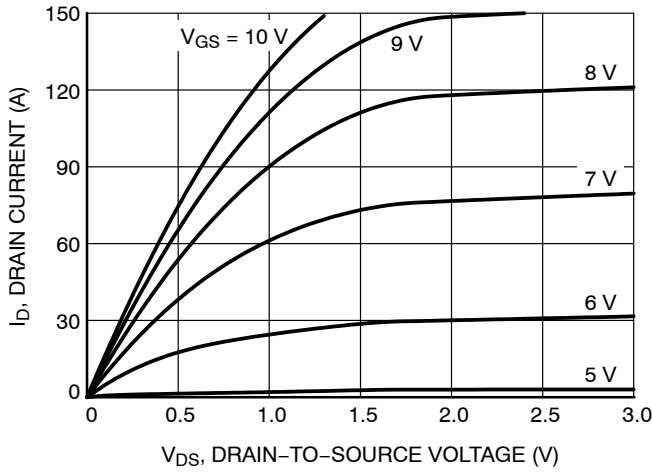


Figure 1. On-Region Characteristics

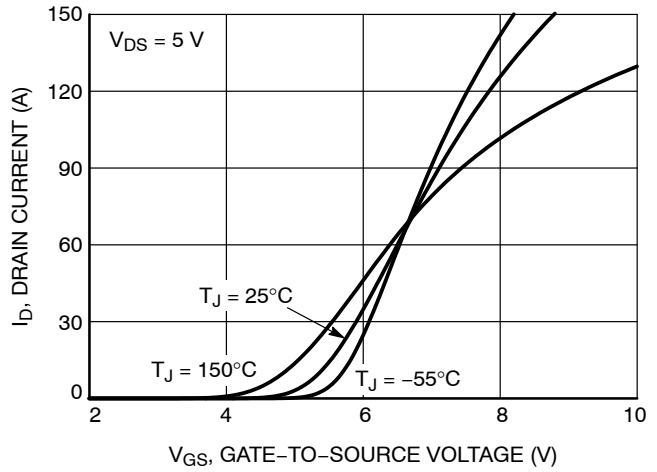


Figure 2. Transfer Characteristics

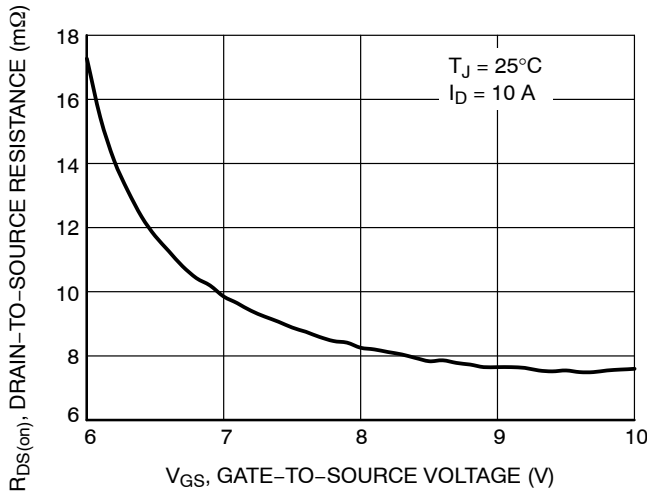


Figure 3. On-Resistance vs. Gate-to-Source Voltage

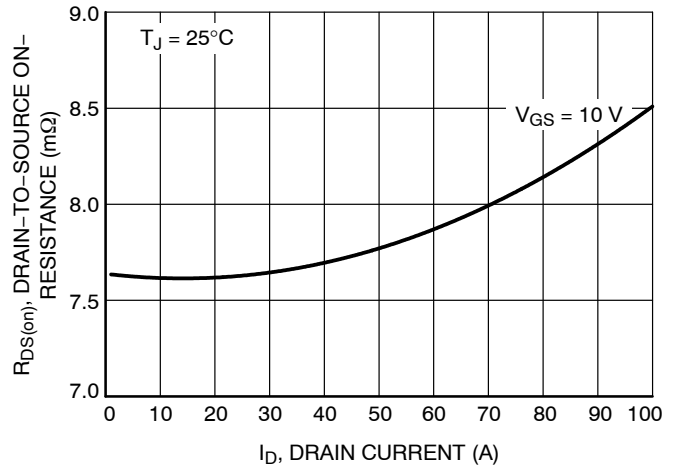


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

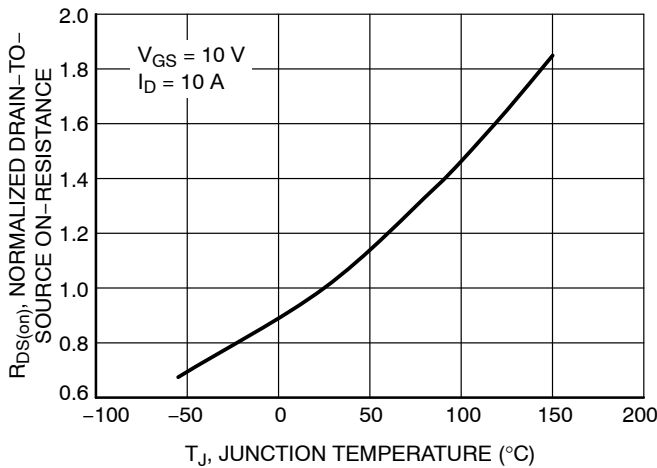


Figure 5. On-Resistance Variation with Temperature

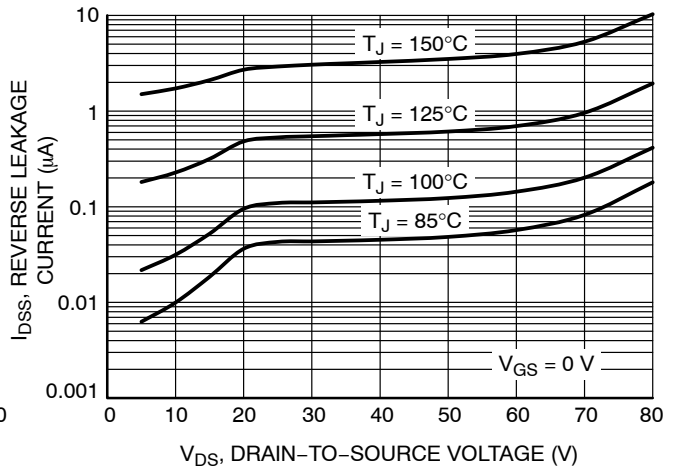


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

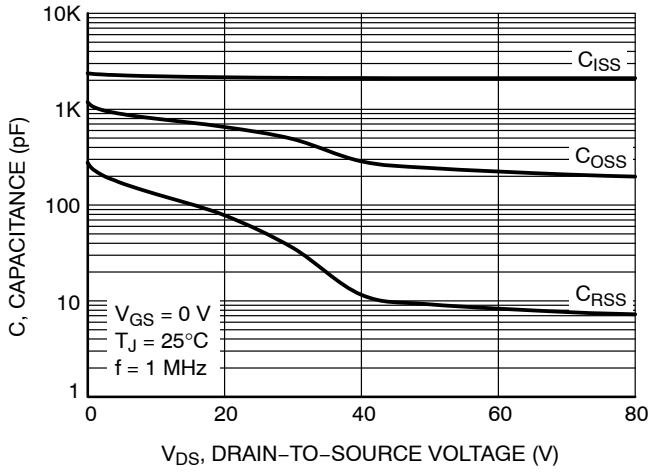


Figure 7. Capacitance Variation

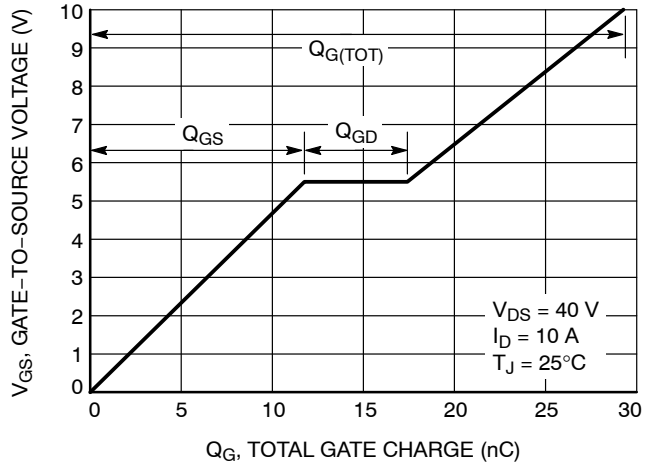


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

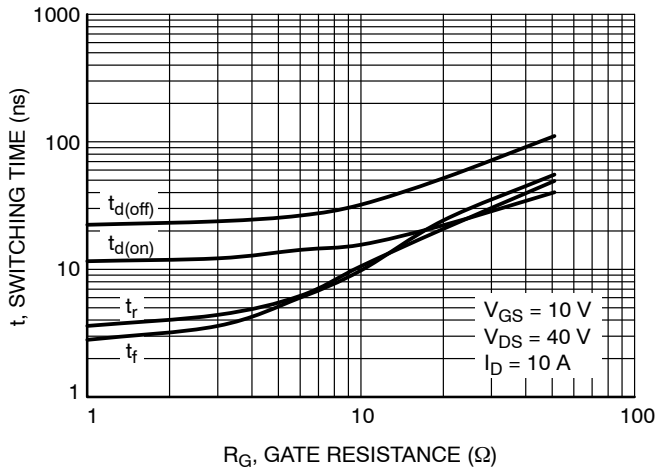


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

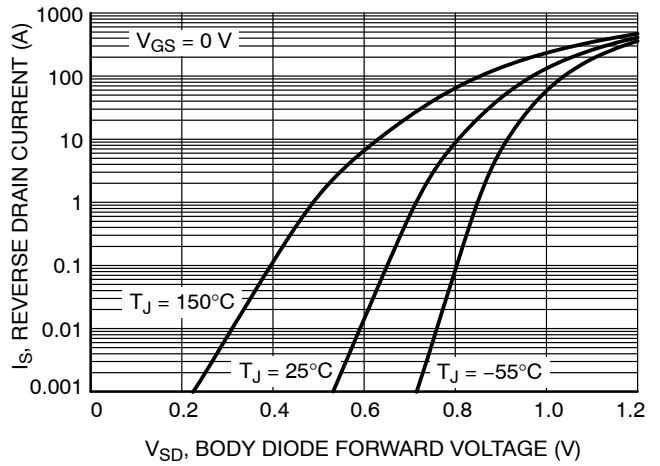


Figure 10. Diode Forward Voltage vs. Current

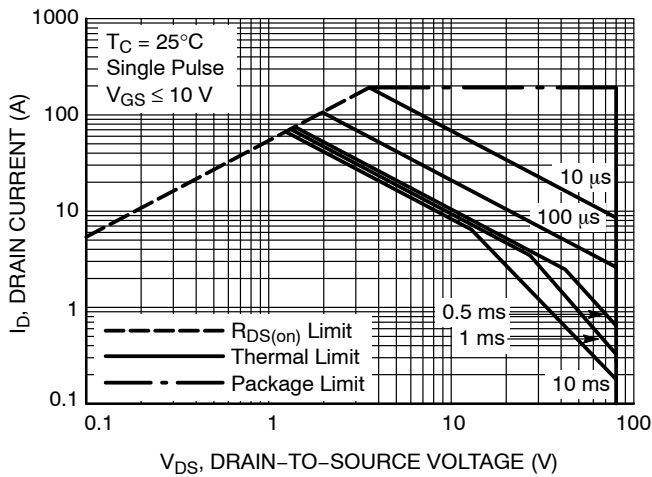


Figure 11. Safe Operating Area

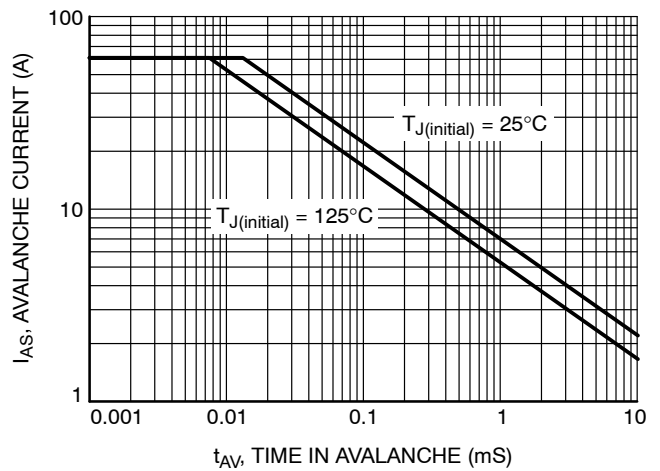


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

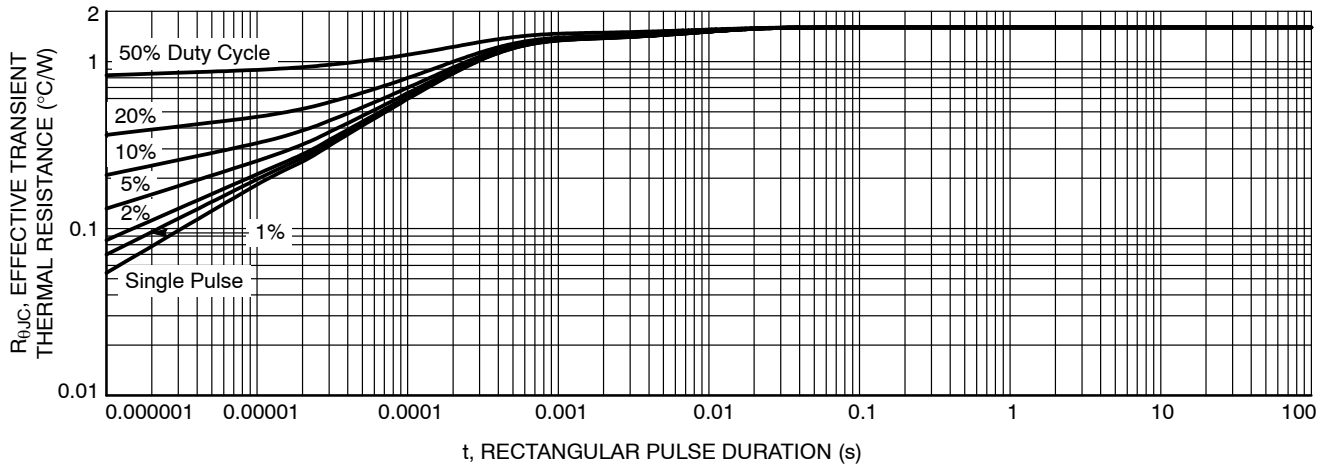


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE

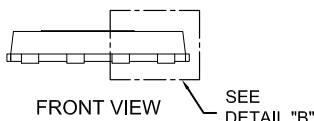
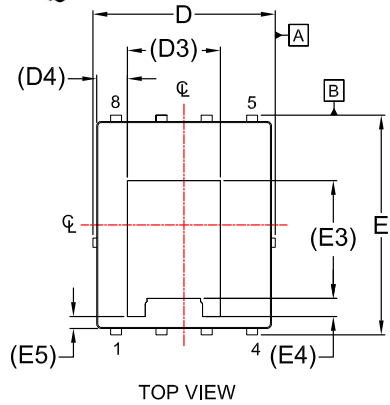
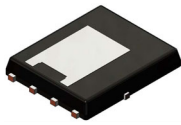
PACKAGE DIMENSIONS

ON Semiconductor®



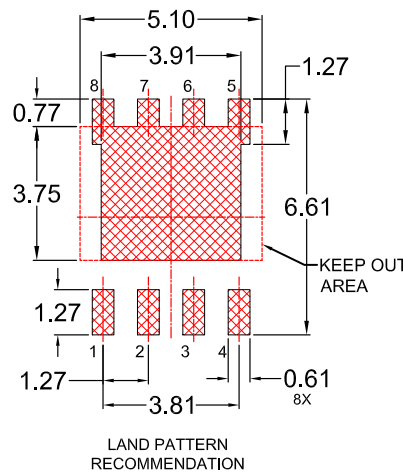
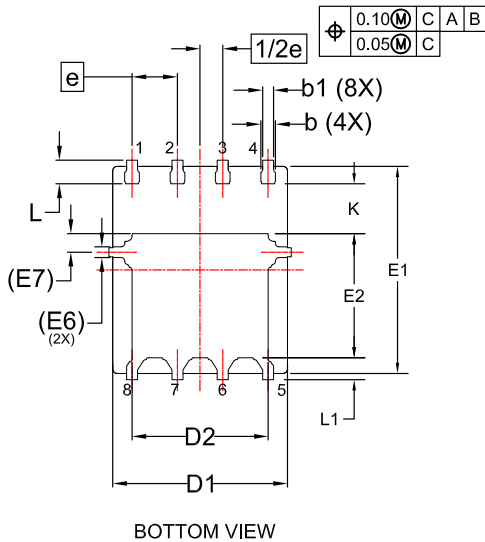
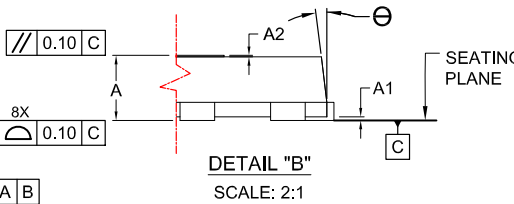
DFN8 5x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D

DATE 25 AUG 2020



NOTES:

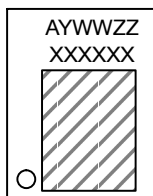
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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