MOSFET - Power, Single N-Channel, PQFN8

100 V, 7.6 mΩ, 110 A

NTMFS7D8N10G

V_{SSS}	$R_{SS(ON)}$ MAX	I_D MAX
100 V	7.6 mΩ @ 10 V	110 A

Features

- Wide SOA for Linear Mode Operation
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- High Peak UIS Current Capability for Ruggedness
- Small Footprint (5x6 mm) for Compact Design
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- 48 V Hot Swap System, Load Switch, Soft Start, E−Fuse

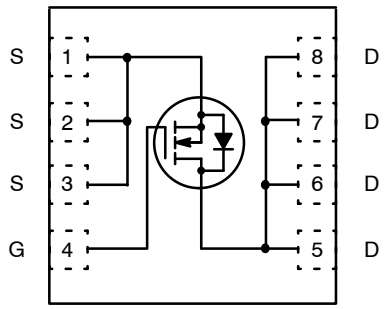
MAXIMUM RATINGS (T_J = 25°C, Unless otherwise specified)

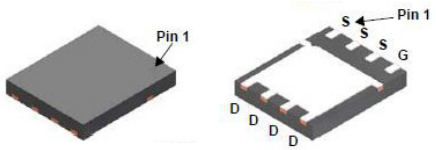
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	T_C = 25°C	I_D	110	A
Power Dissipation $R_{\theta JC}$ (Note 2)			P_D	187	W
Continuous Drain Current $R_{\theta JA}$ (Note 1, 2)	Steady State	T_A = 25°C	I_D	14	A
Power Dissipation $R_{\theta JA}$ (Note 1, 2)			P_D	3	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	1656	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	155	A
Single Pulse Drain−to−Source Avalanche Energy (I_{AV} = 70 A, L = 0.1 mH)			E_{AS}	245	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in^2 pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

N−Channel MOSFET

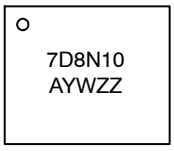




Top Bottom

PQFN8 5x6
CASE 483AF

MARKING DIAGRAM



7D8N10 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction−to−Case − Steady State	0.8	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State	50	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain − to − Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain − to − Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J	I_D = 250 μA, ref to 25°C			87.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			1	μA
			T_J = 125°C			100	
Gate − to − Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 254 μA		2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}$ / T_J	I_D = 254 μA, ref to 25°C			−9.4		mV/°C
Drain − to − Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 48 A			5.6	7.6	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 48 A			37		S
Gate−Resistance	R_G	T_A = 25°C			0.33		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V			6180		pF
Output Capacitance	C_{OSS}				624.5		
Reverse Transfer Capacitance	C_{RSS}				99		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 48 A			92		nC
Gate−to−Source Charge	Q_{GS}				35		
Gate−to−Drain Charge	Q_{GD}				26		
Plateau Voltage	V_{GP}				6		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn − On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 48 A, R_G = 4.7 Ω			32		ns
Rise Time	t_r				24		
Turn − Off Delay Time	$t_{d(OFF)}$				51		
Fall Time	t_f				14		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 48 A	T_J = 25°C		0.84		V
			T_J = 125°C		0.73		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 300 A/μs, I_S = 24 A			42		ns
Reverse Recovery Charge	Q_{RR}				177		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 1000 A/μs, I_S = 24 A			33		ns
Reverse Recovery Charge	Q_{RR}				411		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

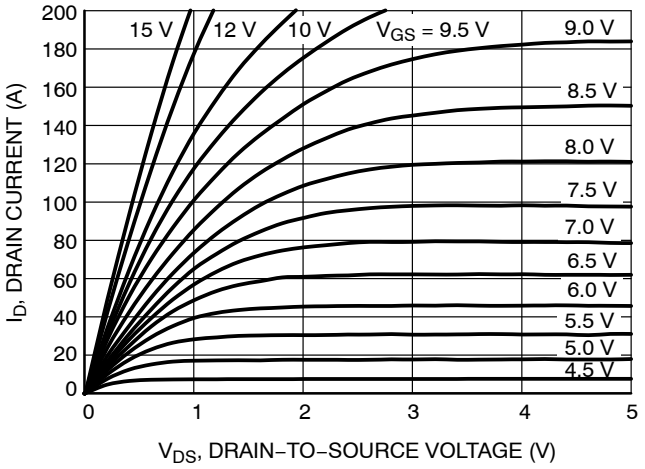


Figure 1. On−Region Characteristics

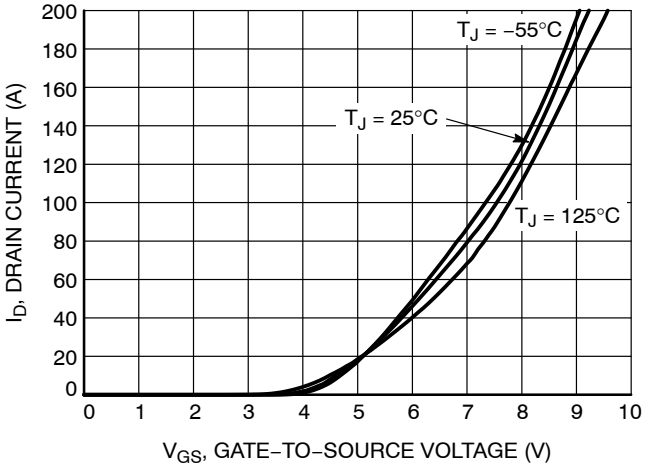


Figure 2. Transfer Characteristics

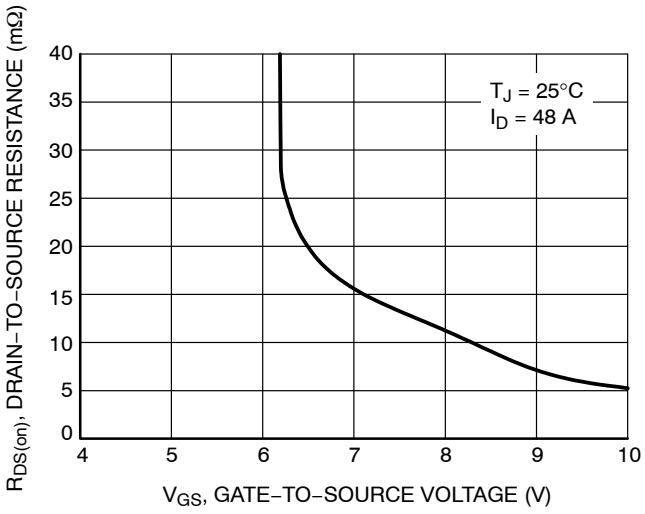


Figure 3. On−Resistance vs. Gate−to−Source Voltage

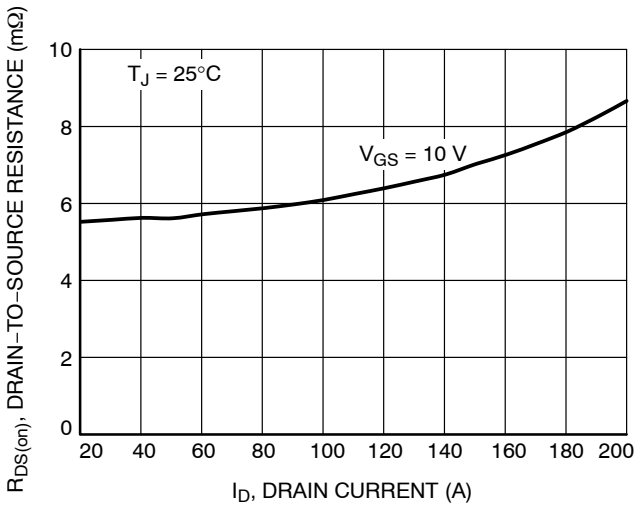


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

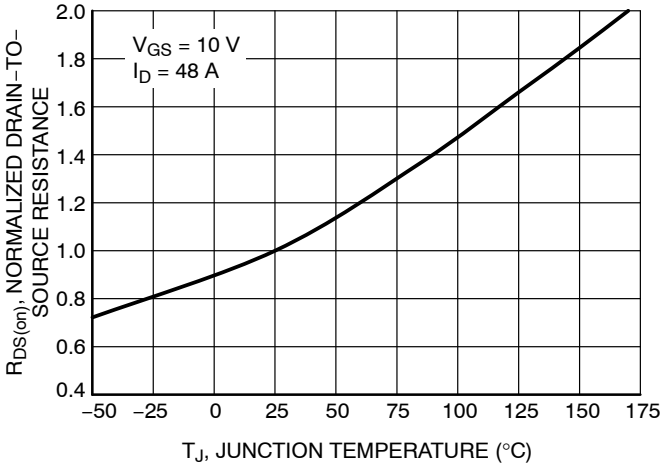


Figure 5. On−Resistance Variation with Temperature

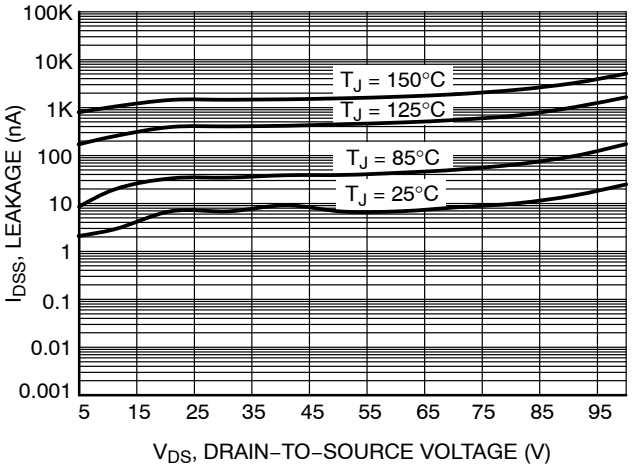


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

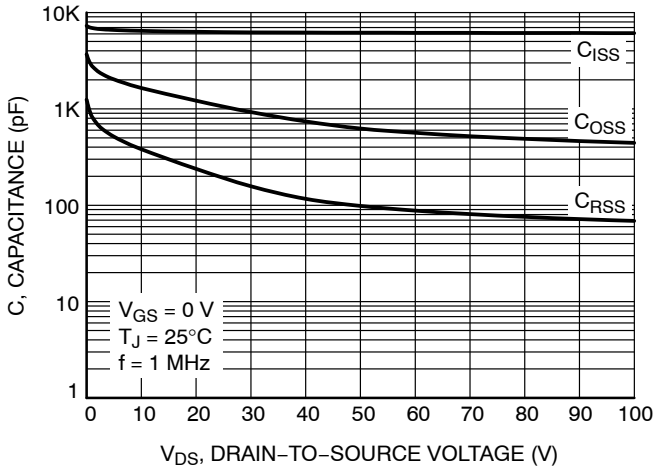


Figure 7. Capacitance Variation

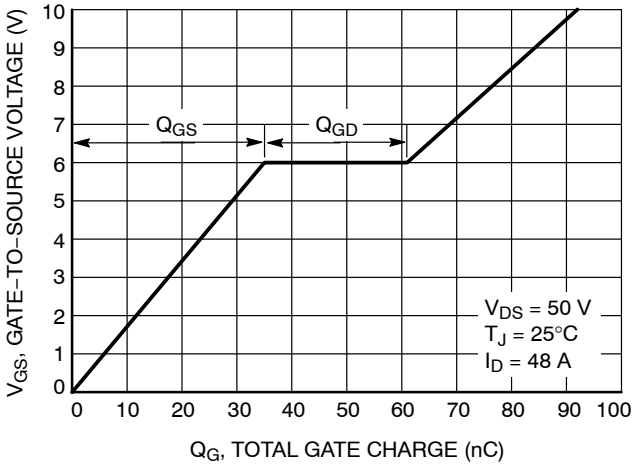


Figure 8. Gate−to−Source Voltage vs. Total Charge

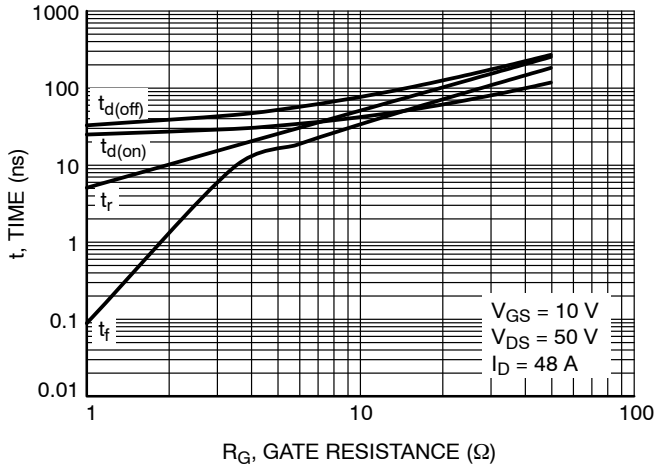


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

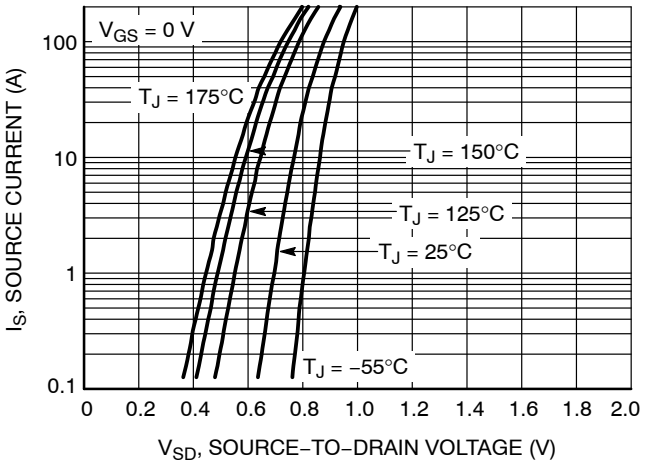


Figure 10. Diode Forward Voltage vs. Current

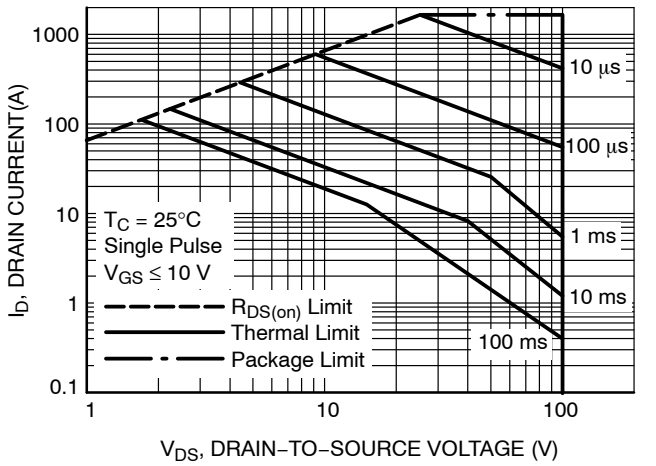


Figure 11. Maximum Rated Forward Biased Safe Operating Area

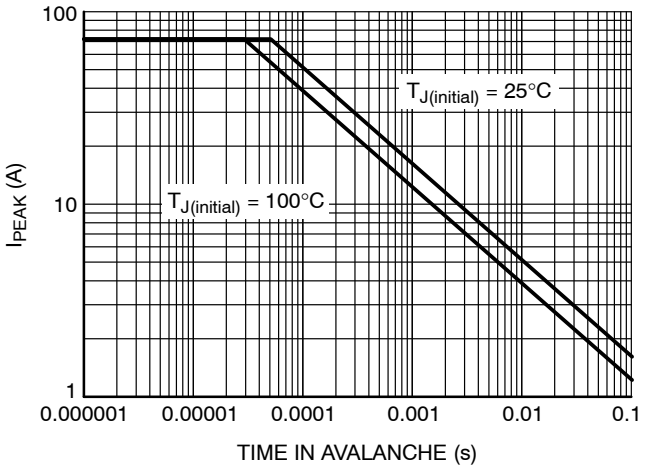


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

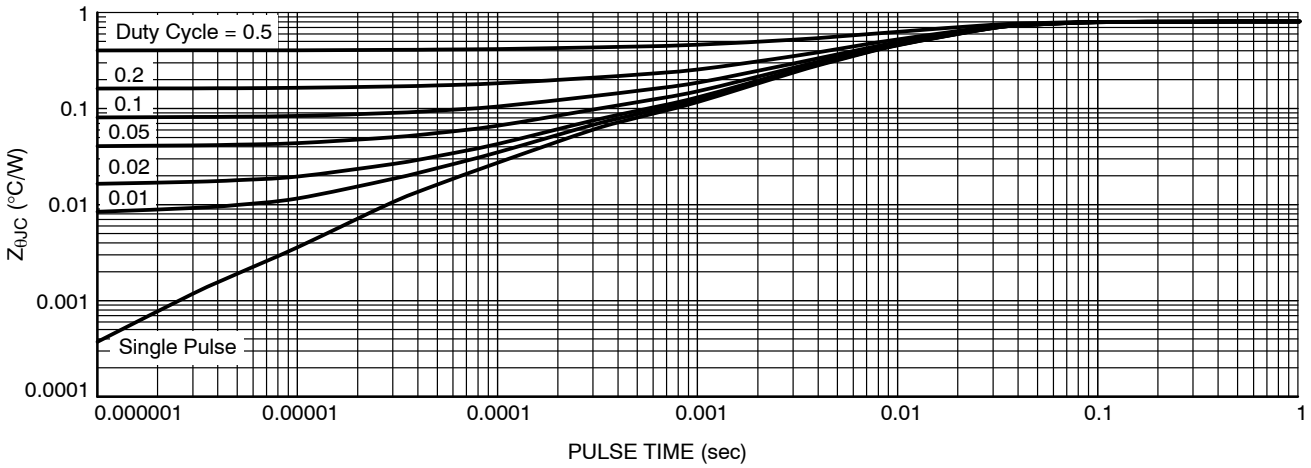
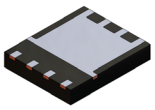


Figure 13. Thermal Characteristics

ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
NTMFS7D8N10GTWG	7D8N10	PQFN8 5x6 (Pb−Free/Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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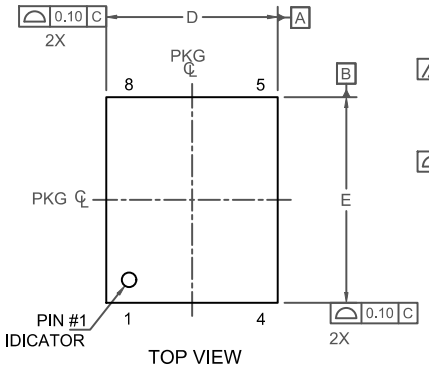
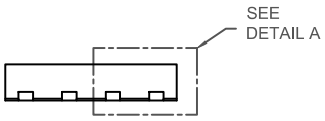
ISSUE A

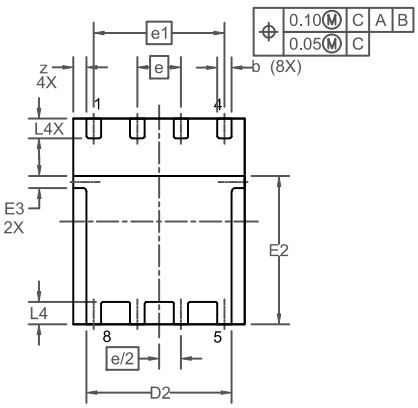
DATE 06 JUL 2021



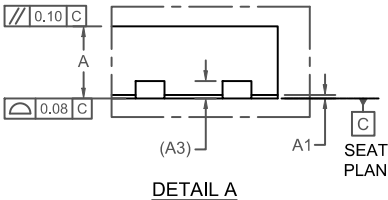
TOP VIEW



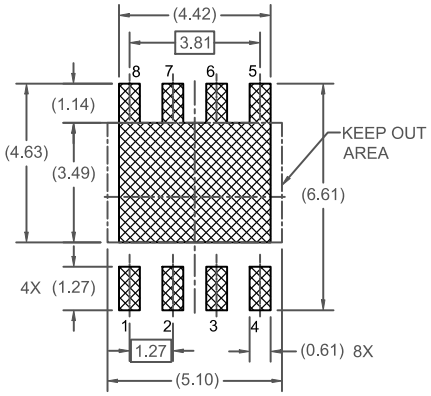
SIDE VIEW



BOTTOM VIEW



DETAIL A
SCALE: 2:1



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF.		
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	4.23	4.33	4.43
E3	0.35 REF.		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
L	0.52	0.57	0.62
L4	0.55	0.65	0.75
z	0.38 REF		

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DESCRIPTION:	**PQFN8 5X6, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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onsemi Website: www.onsemi.com

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