

# MOSFET – N-Channel Shielded Gate POWERTRENCH®

**150 V, 61 A, 14 mΩ**

## NTMFS015N15MC

### Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

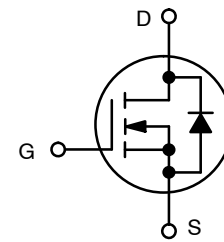
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit
$V_{DSS}$	Drain-to-Source Voltage		150	V
$V_{GS}$	Gate-to-Source Voltage		$\pm 20$	V
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State $T_C = 25^\circ\text{C}$	61	A
$P_D$	Power Dissipation $R_{\theta JC}$ (Note 2)		108.7	W
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State $T_A = 25^\circ\text{C}$	9.2	A
$P_D$	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		2.5	W
$I_{DM}$	Pulsed Drain Current	$T_C = 25^\circ\text{C}$ , $t_p = 100 \mu\text{s}$	302	A
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 10 A_{pk}$ , $L = 3 \text{ mH}$ )		150	mJ
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

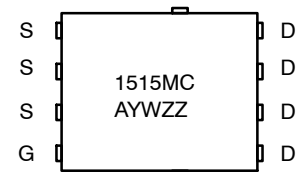
1. Surface-mounted on FR4 board using a 1 in<sup>2</sup>, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
150 V	14 mΩ @ 10 V	61 A



N-CHANNEL MOSFET

### MARKING DIAGRAM



1515MC = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS015N15MC (Pb-Free/Halogen Free)	Power 56 (PQFN8)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# NTMFS015N15MC

## THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	1.15	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Notes 1, 2)	50	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		109		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$			1.0	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 162\ \mu\text{A}$	2.5		4.5	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient	$I_D = 162\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-7.6		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$		10.2	14	m $\Omega$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 8\text{ V}, I_D = 15\text{ A}$		11.1	16.2	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 29\text{ A}$		56		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		2120		pF
$C_{OSS}$	Output Capacitance			595		
$C_{RSS}$	Reverse Transfer Capacitance			10.5		
$R_G$	Gate-Resistance			0.6	1.2	$\Omega$
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 29\text{ A}$		27		nC
$Q_{G(TH)}$	Threshold Gate Charge			7		
$Q_{GS}$	Gate-to-Source Charge			11		
$Q_{GD}$	Gate-to-Drain Charge			4		
$V_{GP}$	Plateau Voltage			5.5		
$Q_{OSS}$	Output Charge	$V_{DD} = 75\text{ V}, V_{GS} = 0\text{ V}$		66		nC

### SWITCHING CHARACTERISTICS (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 29\text{ A}, R_G = 6\ \Omega$		16		ns
$t_r$	Rise Time			5		
$t_{d(OFF)}$	Turn-Off Delay Time			21		
$t_f$	Fall Time			4		

### DRAIN-SOURCE DIODE CHARACTERISTICS

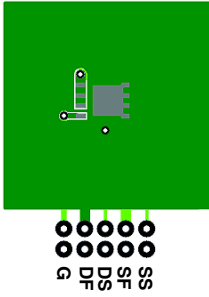
$V_{SD}$	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 29\text{ A}$	$T_J = 25^\circ\text{C}$		0.86	1.2	V
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 300\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			49		ns
$Q_{RR}$	Reverse Recovery Charge					197	
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			34		ns
$Q_{RR}$	Reverse Recovery Charge					345	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

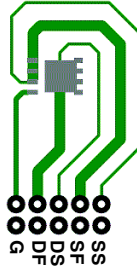
# NTMFS015N15MC

## NOTES:

3. Switching characteristics are independent of operating junction temperatures.
4.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

TYPICAL CHARACTERISTICS

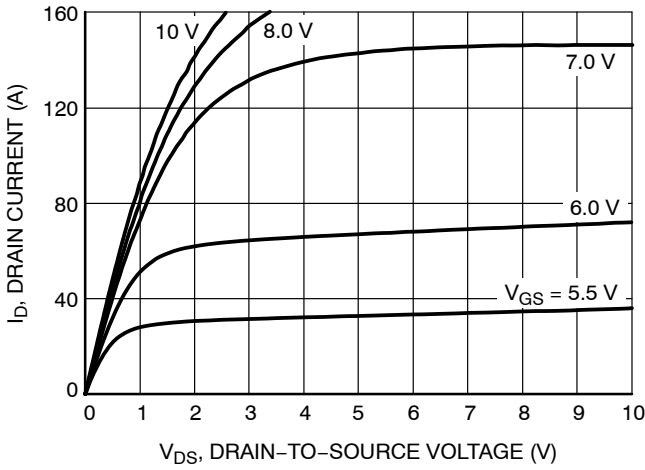


Figure 1. On-Region Characteristics

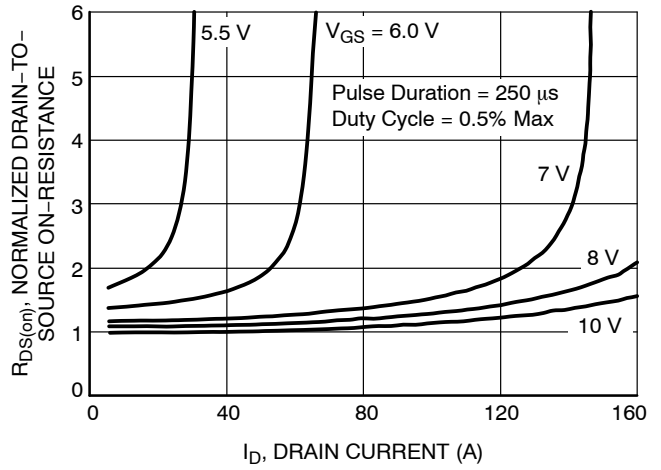


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

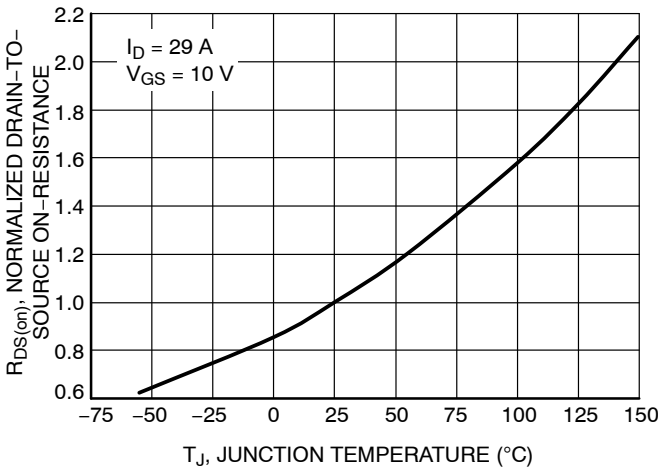


Figure 3. Normalized On-Resistance vs. Junction Temperature

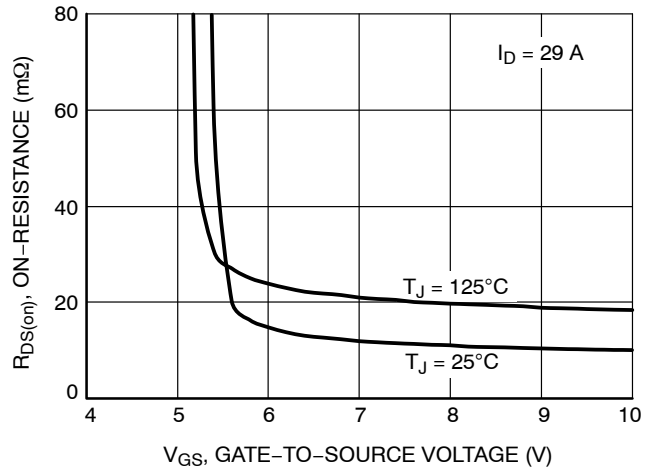


Figure 4. On-Resistance vs. Gate-to-Source Voltage

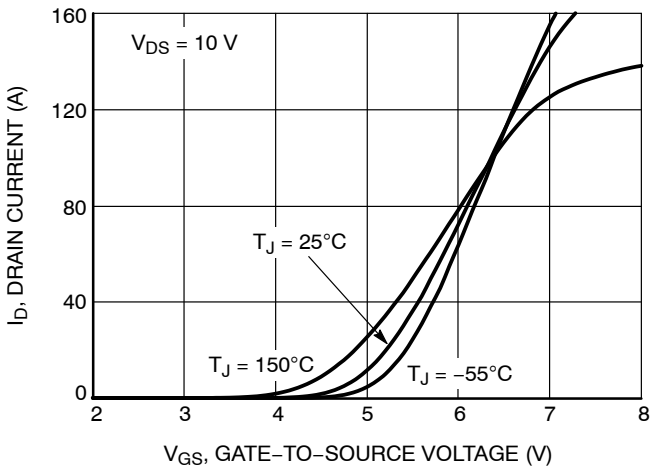


Figure 5. Transfer Characteristics

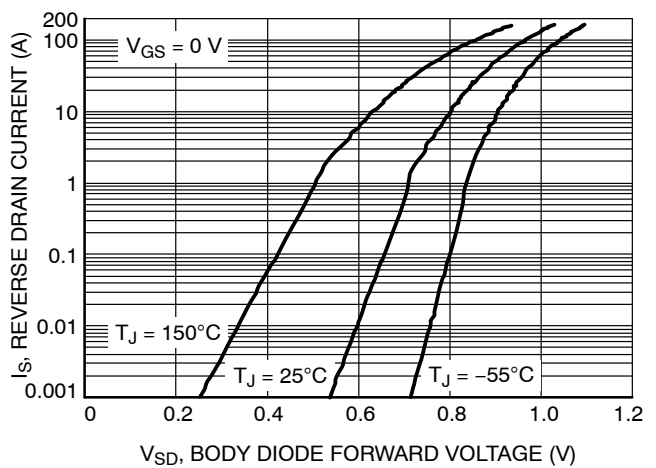
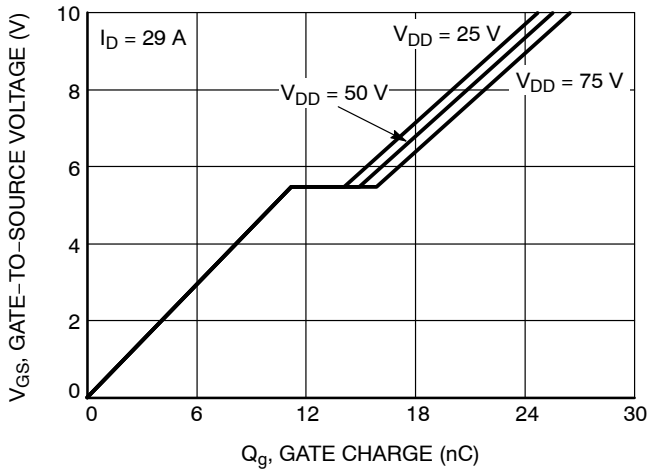
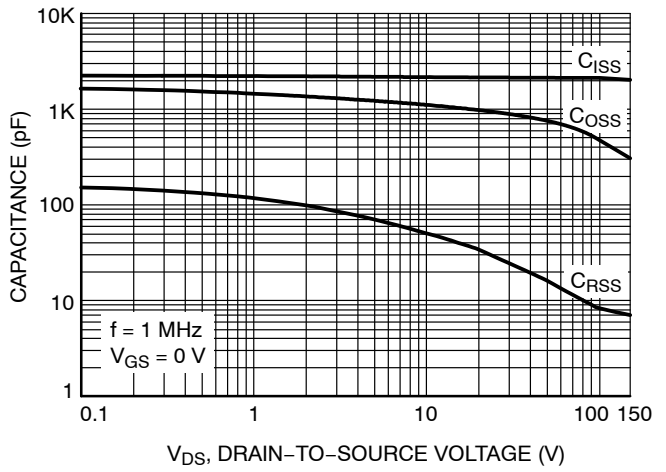


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

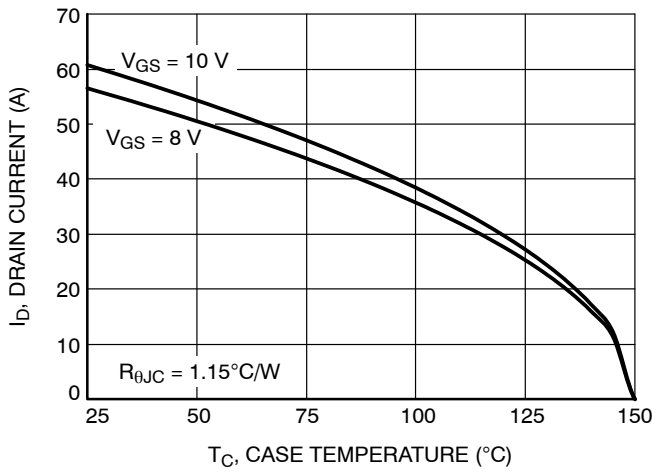
## TYPICAL CHARACTERISTICS (continued)



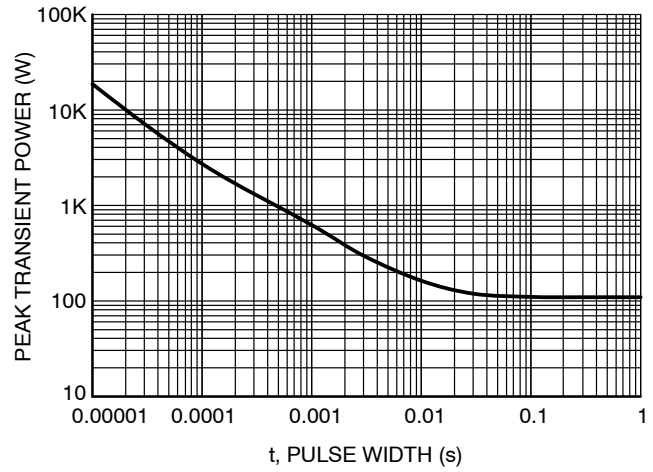
**Figure 7. Gate Charge Characteristics**



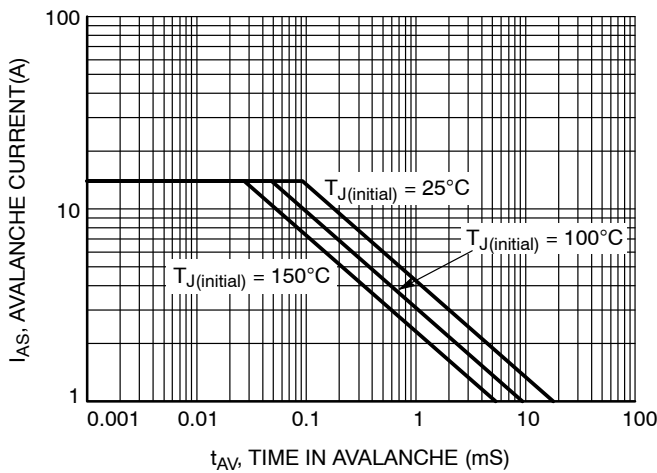
**Figure 8. Capacitance vs. Drain-to-Source Voltage**



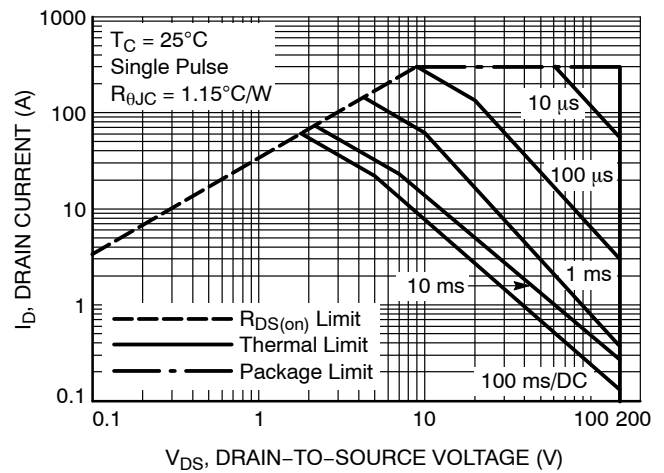
**Figure 9. Drain Current vs. Case Temperature**



**Figure 10. Peak Power**



**Figure 11. Unclamped Inductive Switching Capability**



**Figure 12. Forward Bias Safe Operating Area**

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## TYPICAL CHARACTERISTICS (continued)

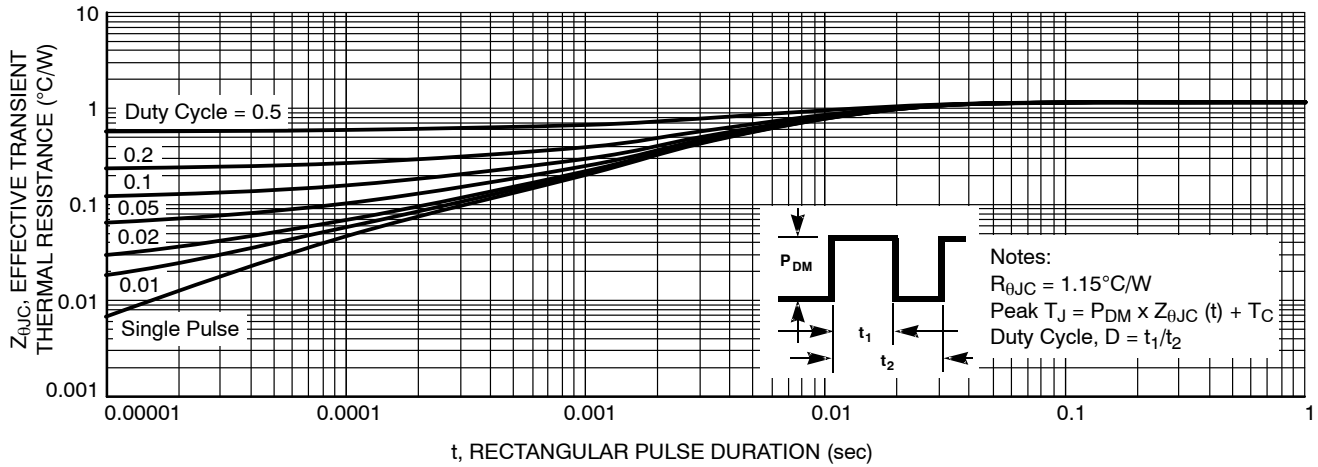
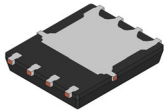
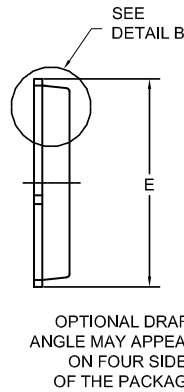
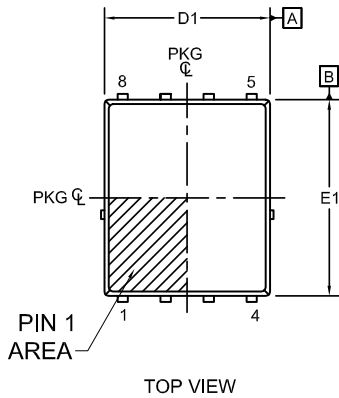


Figure 13. Transient Thermal Impedance



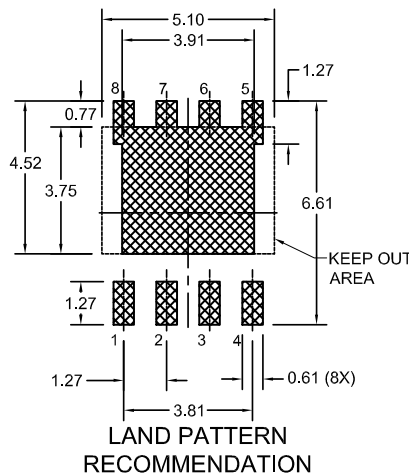
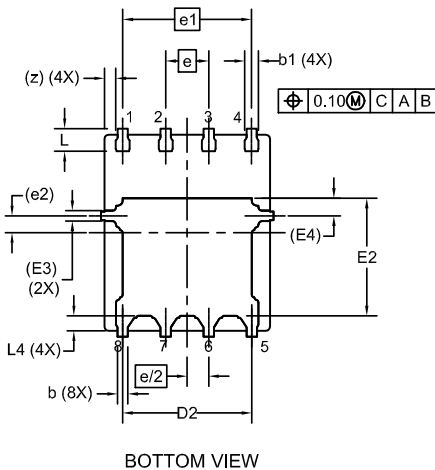
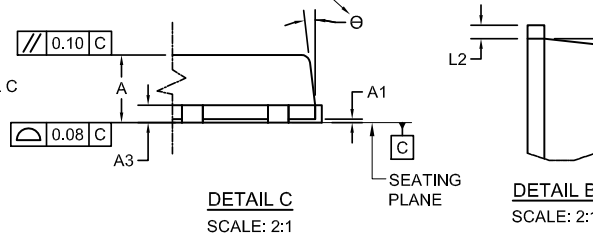
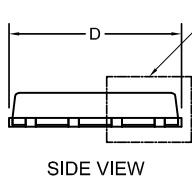
**PQFN8 5X6, 1.27P**  
**CASE 483AE**  
**ISSUE C**

DATE 21 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



**LAND PATTERN RECOMMENDATION**  
 \*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°

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