ON Semiconductor

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MOSFET - Power, Single P-Channel, SO8-FL -30 V, 2.7 m Ω , -164 A

-30 V, 2.7 III.2, -104 A

NTMFS005P03P8Z

Features

- Ultra Low R_{DS(on)} to Improve System Efficiency
- Advanced Package Technology in 5x6mm for Space Saving and Excellent Thermal Conduction
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-30	V
Gate-to-Source Voltage			V_{GS}	±25	V
Continuous Drain		T _C = 25°C	I _D	-164	Α
Current R _{θJC} (Note 3)	Steady	T _C = 85°C		-118	
Power Dissipation $R_{\theta JC}$ (Note 3)	State	T _C = 25°C	P _D	104	W
Continuous Drain Cur-		T _A = 25°C	I _D	-28.6	Α
rent R _{θJA} (Notes 1, 3)	Steady	T _A = 85°C		-20.6	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	State	T _A = 25°C	P _D	3.2	W
Continuous Drain Cur-		T _A = 25°C	I _D	-15.3	Α
rent $R_{\theta JA}$ (Notes 2, 3)	Steady	T _A = 85°C		-11	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	State	T _A = 25°C	P _D	0.9	W
Pulsed Drain Current	in Current $T_A = 25$ °C, $t_p = 10$ μs			-597	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{Lpk} = 57.59 A)			E _{AS}	165.8	mJ
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

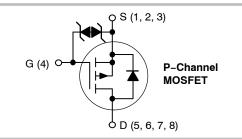
- 1. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz. Cu pad.
- 2. Surface-mounted on FR4 board using a minimum pad size, 2 oz. Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

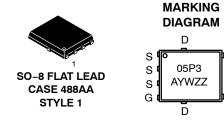


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V _{(BR)DSS}	R _{DS(on)}	I _D
-30 V	2.7 mΩ @ –10 V	-164 A
	4.4 mΩ @ –4.5 V	-10 4 A





A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFS005P03P8ZT1G	SO8-FL (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Drain) (Note 1)	$R_{\theta JC}$	1.2	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	40	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	137	°C/W

ELECTRICAL CHARACTERISTICS (T₁ = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•		•			•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V_{GS} = 0 V, I_D = -250 μA		-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J	I _D = -250 μA, re	f to 25°C		-8.3		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -24 V	T _J = 25°C			-1.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	= ±25 V			±10	μΑ
ON CHARACTERISTICS (Note 4)							-
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D =$	-250 μΑ	-1.0		-3.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J	I _D = -250 μA, re	of to 25°C		5.3		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D$	= -22 A		1.8	2.7	mΩ
		V _{GS} = -4.5 V, I _C	₀ = -16 A		2.9	4.4	1
Froward Transconductance	9FS	V _{DS} = -5 V, I _D = -16 A			87		S
CHARGES AND CAPACITANCES	•		•			•	
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = -15 \text{ V},$ f = 1.0 MHz			7880		pF
Output Capacitance	C _{oss}				2630		
Reverse Transfer Capacitance	C _{rss}				2550		
Total Gate Charge	Q _{G(TOT)}				112		nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = -4.5 \text{ V}, V_{DS} = -15 \text{ V},$ $I_{D} = -22 \text{ A}$ $V_{GS} = -10 \text{ V}, V_{DS} = -15 \text{ V},$ $I_{D} = -22 \text{ A}$			8		-
Gate-to-Source Charge	Q_{GS}				16		
Gate-to-Drain Charge	Q_{GD}				76		
Total Gate Charge	Q _{G(TOT)}				183		1
SWITCHING CHARACTERISTICS, Vo	as = 4.5 V (Note	4)	•			•	•
Turn-On Delay Time	t _{d(on)}				56		ns
Rise Time	t _r	$V_{GS} = -4.5 \text{ V}, V_{DS}$	s = -15 V.		308		-
Turn-Off Delay Time	t _{d(off)}	$I_D = -22 A, R_C$			124		
Fall Time	t _f				269		1
SWITCHING CHARACTERISTICS, V _C	as = 10 V (Note 4	.)					
Turn-On Delay Time	t _{d(on)}	V_{GS} = -10 V, V_{DS} = -15 V, I_{D} = -22 A, R_{G} = 6 Ω			22		ns
Rise Time	t _r				79		
Turn-Off Delay Time	t _{d(off)}				220		
Fall Time	t _f				258		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS		<u> </u>				•
Forward Diode Voltage	de Voltage V _{SD}	V _{GS} = 0 V,	T _J = 25°C		-0.77	-1.3	V
	$I_S = -22 A$	$I_S = -22 \text{ A}$ $T_J = 125^{\circ}\text{C}$		-0.63		1	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit	
DRAIN-SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dl_{S}/dt = 100 \text{ A}/\mu\text{s,}$ $l_{s} = -22 \text{ A}$		57		ns	
Charge Time	ta			34			
Discharge Time	t _b			23			
Reverse Recovery Charge	Q _{RR}			77		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

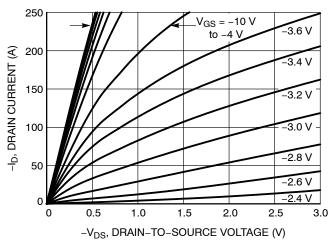


Figure 1. On-Region Characteristics

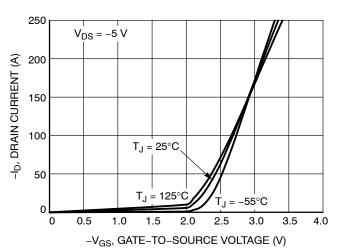


Figure 2. Transfer Characteristics

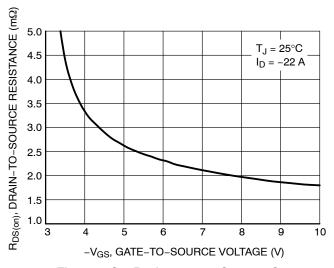


Figure 3. On-Resistance vs. Gate-to-Source Voltage

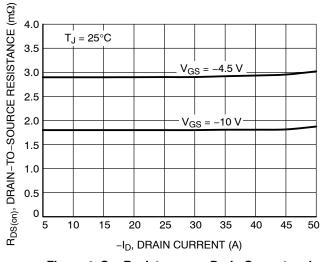


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

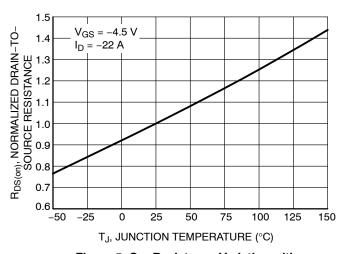


Figure 5. On–Resistance Variation with Temperature

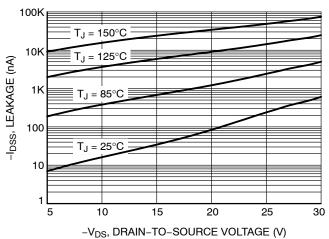


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

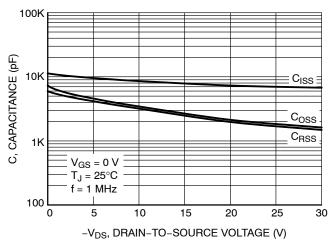


Figure 7. Capacitance Variation

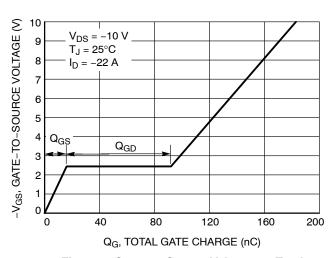


Figure 8. Gate-to-Source Voltage vs. Total Charge

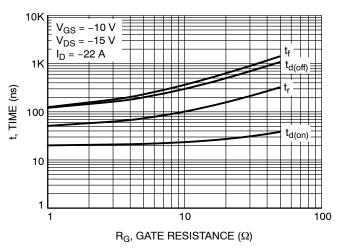


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

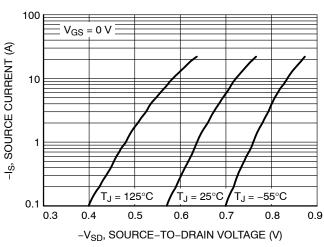


Figure 10. Diode Forward Voltage vs. Current

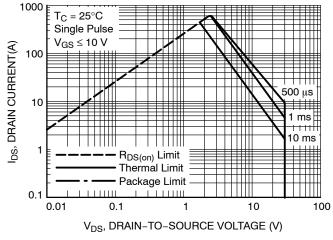


Figure 11. Maximum Rated Forward Biased Safe Operating Area

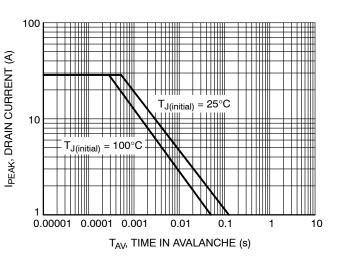


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

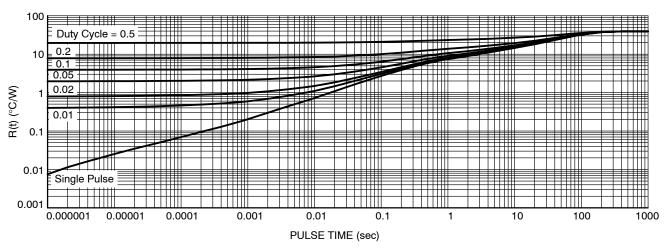
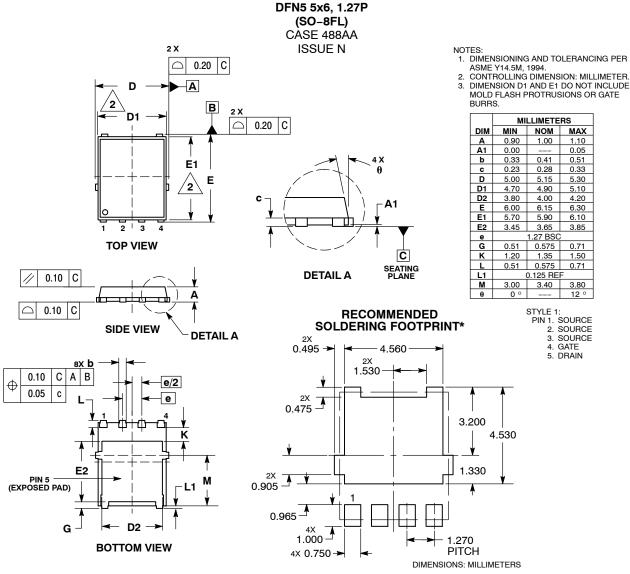


Figure 13. Thermal Characteristics

PACKAGE DIMENSIONS



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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