

# NTMFD4901NF

## MOSFET – Power, Dual, N-Channel with Integrated Schottky, SO8FL

30 V, High Side 18 A / Low Side 30 A

### Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Low Side MOSFET with Integrated Schottky
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

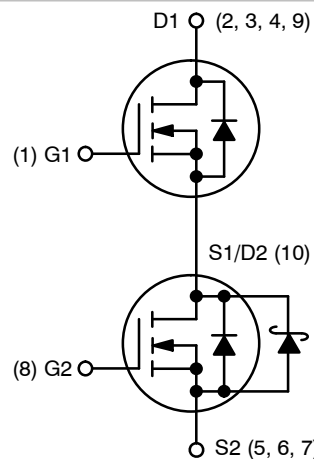
- DC-DC Converters
- System Voltage Rails
- Point of Load



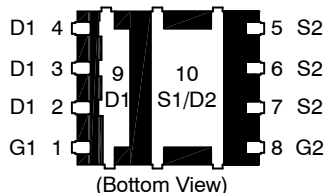
ON Semiconductor®

<http://onsemi.com>

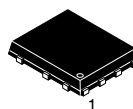
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
Q1 Top FET 30 V	6.5 mΩ @ 10 V	18 A
	10 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	2.35 mΩ @ 10 V	30 A
	3.5 mΩ @ 4.5 V	



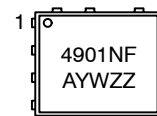
### PIN CONNECTIONS



### MARKING DIAGRAM



DFN8  
CASE 506BX



4901NF = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTMFD4901NF

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage	Q1	$V_{DSS}$	30	V	
Drain-to-Source Voltage	Q2				
Gate-to-Source Voltage	Q1	$V_{GS}$	$\pm 20$	V	
Gate-to-Source Voltage	Q2				
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$T_A = 25^\circ\text{C}$	Q1	13.5	A	
		Q2	23.4		
	$T_A = 85^\circ\text{C}$	Q1	9.7		
		Q2	16.9		
Power Dissipation $R_{\theta JA}$ (Note 1)	$T_A = 25^\circ\text{C}$	Q1	1.90	W	
		Q2	2.07		
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	$T_A = 25^\circ\text{C}$	Q1	18.2	A	
		Q2	30.3		
	$T_A = 85^\circ\text{C}$	Q1	13.1		
		Q2	21.8		
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	$T_A = 25^\circ\text{C}$	Q1	3.45	W	
		Q2	3.45		
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$T_A = 25^\circ\text{C}$	Q1	10.3	A	
		Q2	17.9		
	$T_A = 85^\circ\text{C}$	Q1	7.4		
		Q2	12.9		
Power Dissipation $R_{\theta JA}$ (Note 2)	$T_A = 25^\circ\text{C}$	Q1	1.10	W	
		Q2	1.20		
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ $t_p = 10 \mu\text{s}$	Q1	60	A	
		Q2	100		
Operating Junction and Storage Temperature	Q1	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$	
	Q2				
Source Current (Body Diode)	Q1	$I_S$	3.4	A	
	Q2		4.9		
Drain to Source $dV/dt$		$dV/dt$	6	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = XX$ A <sub>pk</sub> , $L = 0.1$ mH, $R_G = 25 \Omega$ )	24 A	Q1	EAS	28.8	mJ
	48 A	Q2	EAS	115	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm<sup>2</sup>.

# NTMFD4901NF

## THEMAL RESISTANCE MAXIMUM RATINGS

Parameter	FET	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	Q1	R <sub>θJA</sub>	65.9	°C/W
	Q2		60.5	
Junction-to-Ambient – Steady State (Note 4)	Q1	R <sub>θJA</sub>	113.2	
	Q2		104	
Junction-to-Ambient – (t ≤ 10 s) (Note 3)	Q1	R <sub>θJA</sub>	36.2	
	Q2		36.2	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm<sup>2</sup>.

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>							
Drain-to-Source Break-down Voltage	Q1	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
	Q2		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	30			
Drain-to-Source Break-down Voltage Temperature Coefficient	Q1	V <sub>(BR)DSS</sub> / T <sub>J</sub>			18		mV / °C
	Q2				15		
Zero Gate Voltage Drain Current	Q1	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		1	μA
				T <sub>J</sub> = 125°C		10	
	Q2		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		500	
Gate-to-Source Leakage Current	Q1	I <sub>GSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = ±20 V			±100	nA
	Q2					±100	

## ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	Q1	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA		1.2		2.2	V
	Q2				1.2		2.2	
Negative Threshold Temperature Coefficient	Q1	V <sub>GS(TH)</sub> / T <sub>J</sub>				4.5		mV / °C
	Q2					4.0		
Drain-to-Source On Resistance	Q1	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A		5.2	6.5	mΩ
			V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 10 A		8.0	10	
	Q2		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A		1.9	2.35	
			V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A		2.8	3.5	
Forward Transconductance	Q1	g <sub>FS</sub>	V <sub>DS</sub> = 1.5 V, I <sub>D</sub> = 10 A			28		S
	Q2					45		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

# NTMFD4901NF

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
<b>CHARGES, CAPACITANCES &amp; GATE RESISTANCE</b>							
Input Capacitance	Q1	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 15 V		1150		pF
	Q2				2950		
Output Capacitance	Q1	C <sub>OSS</sub>			360		
	Q2				1100		
Reverse Capacitance	Q1	C <sub>RSS</sub>			105		
	Q2				82		
Total Gate Charge	Q1	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 10 A		9.7		nC
	Q2				20		
Threshold Gate Charge	Q1	Q <sub>G(TH)</sub>			1.1		
	Q2				2.7		
Gate-to-Source Charge	Q1	Q <sub>GS</sub>			3.3		
	Q2				7.3		
Gate-to-Drain Charge	Q1	Q <sub>GD</sub>			3.7		
	Q2			5.3			
Total Gate Charge	Q1	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 10 A		19.1		nC
	Q2				42.7		

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A, R <sub>G</sub> = 3.0 Ω		9.0		ns
	Q2				14		
Rise Time	Q1	t <sub>r</sub>			15		
	Q2				16		
Turn-Off Delay Time	Q1	t <sub>d(OFF)</sub>			14		
	Q2				25		
Fall Time	Q1	t <sub>f</sub>			4.0		
	Q2				7.0		

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A, R <sub>G</sub> = 3.0 Ω		6.0		ns
	Q2				10		
Rise Time	Q1	t <sub>r</sub>			14		
	Q2				15		
Turn-Off Delay Time	Q1	t <sub>d(OFF)</sub>			17		
	Q2				32		
Fall Time	Q1	t <sub>f</sub>			3.0		
	Q2				5.0		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

# NTMFD4901NF

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>								
Forward Voltage	Q1	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 3\text{ A}$	$T_J = 25^\circ\text{C}$	0.75	1.0	V	
				$T_J = 125^\circ\text{C}$	0.62			
	Q2		$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$	$T_J = 25^\circ\text{C}$	0.45	0.70		
				$T_J = 125^\circ\text{C}$	0.37			
Reverse Recovery Time	Q1	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 3\text{ A}$		23		ns	
	Q2				40			
Charge Time	Q1			ta		12		
	Q2					21		
Discharge Time	Q1			tb		11		
	Q2					19		
Reverse Recovery Charge	Q1	$Q_{RR}$		12		nC		
	Q2			40				

## PACKAGE PARASITIC VALUES

Source Inductance	Q1	$L_S$	$T_A = 25^\circ\text{C}$		0.38		nH
	Q2				0.65		
Drain Inductance	Q1	$L_D$			0.054		nH
	Q2				0.007		
Gate Inductance	Q1	$L_G$			1.5		nH
	Q2				1.5		
Gate Resistance	Q1	$R_G$			0.8		$\Omega$
	Q2				0.8		

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTMFD4901NFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NTMFD4901NFT3G	DFN8 (Pb-Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS – Q1

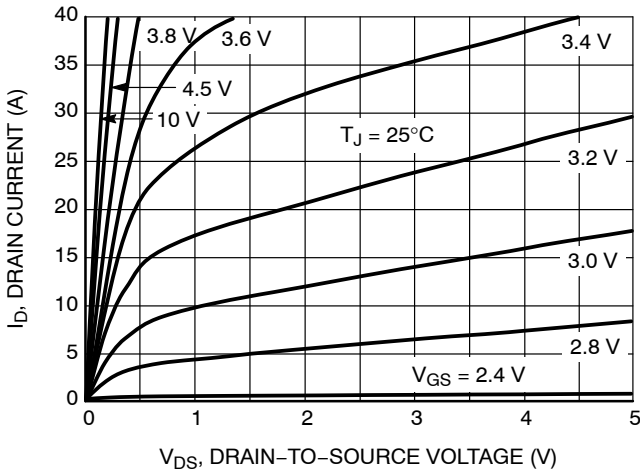


Figure 1. On-Region Characteristics

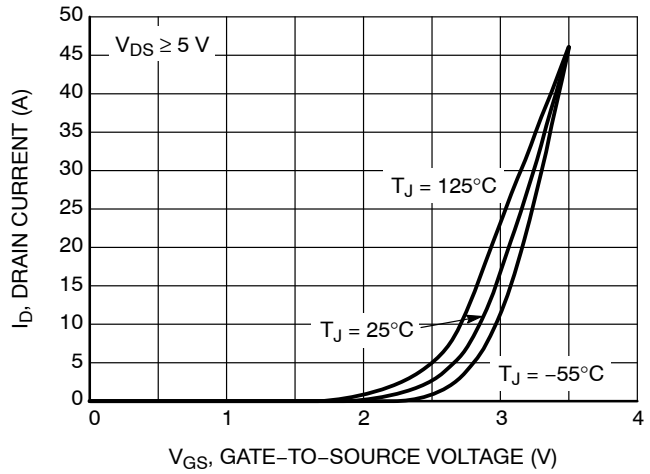


Figure 2. Transfer Characteristics

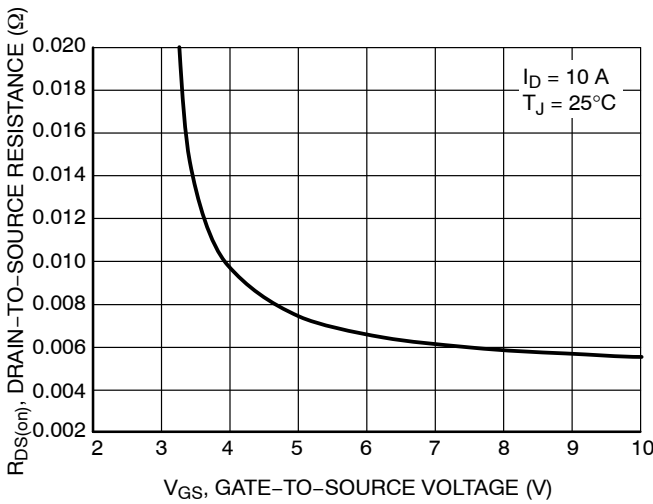


Figure 3. On-Resistance vs. Gate-to-Source Resistance

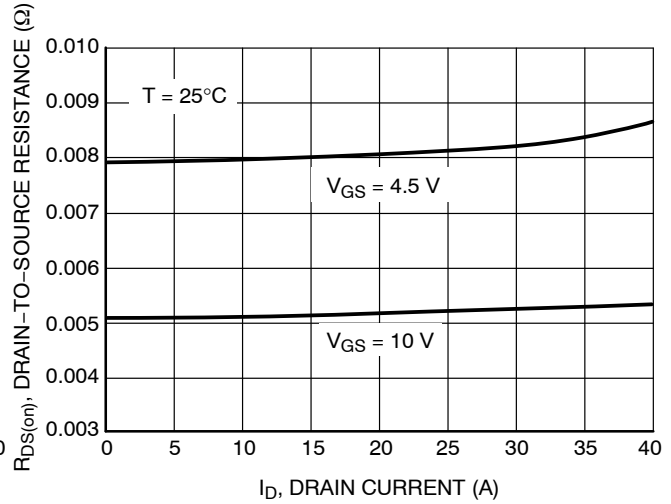


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

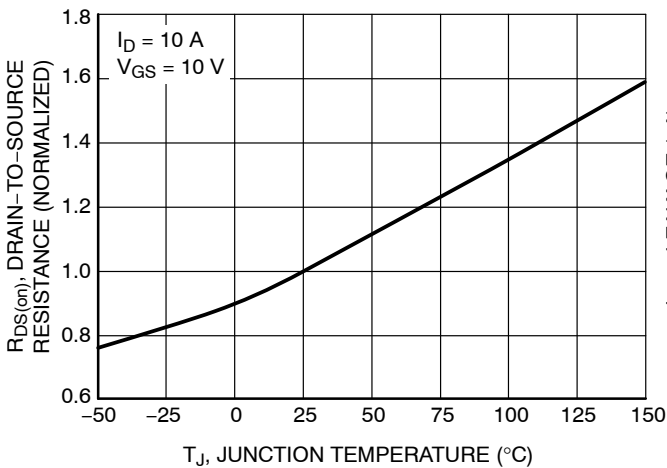


Figure 5. On-Resistance Variation with Temperature

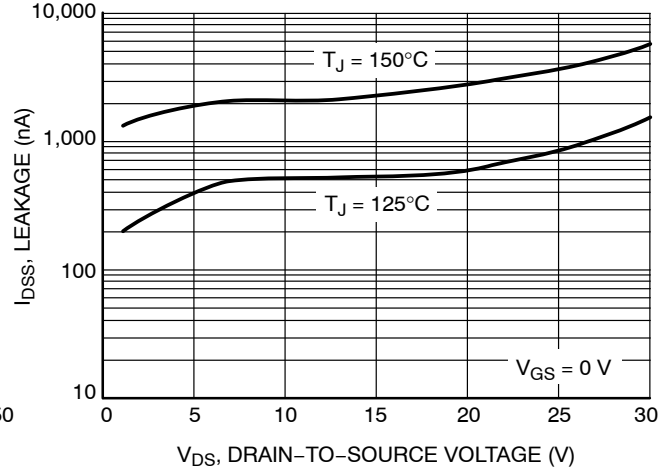


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTMFD4901NF

## TYPICAL CHARACTERISTICS – Q1

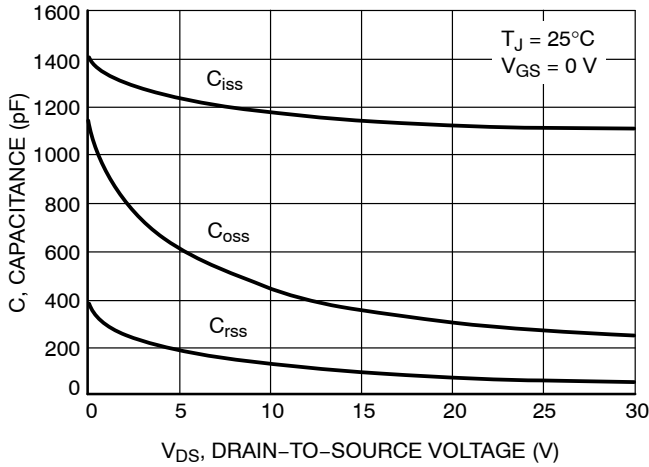


Figure 7. Capacitance Variation

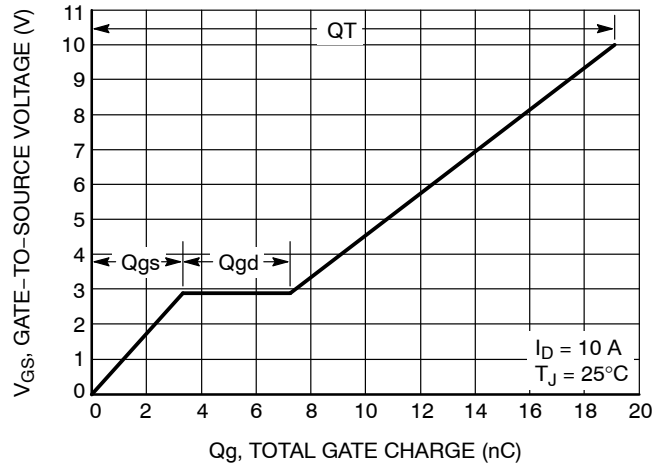


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

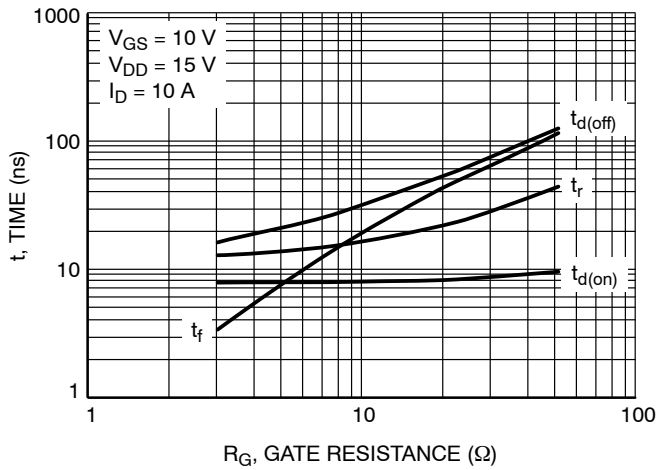


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

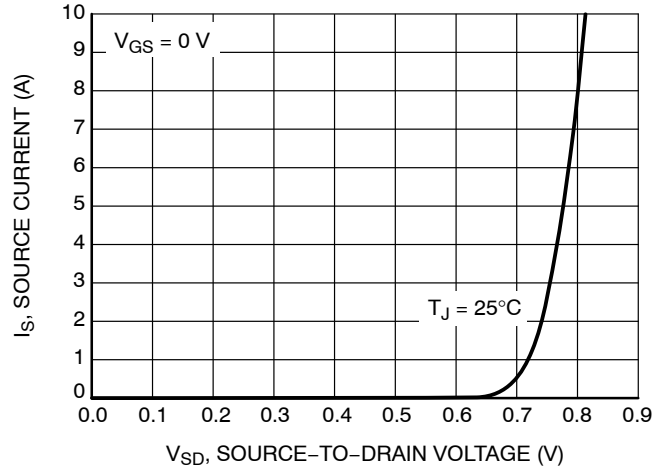


Figure 10. Diode Forward Voltage vs. Current

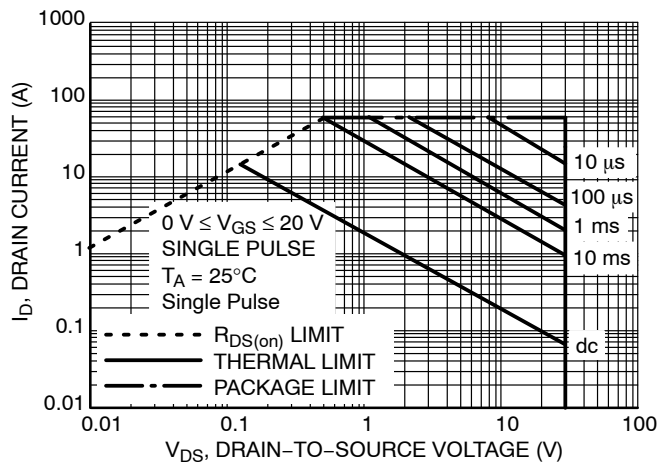


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTMFD4901NF

## TYPICAL CHARACTERISTICS – Q1

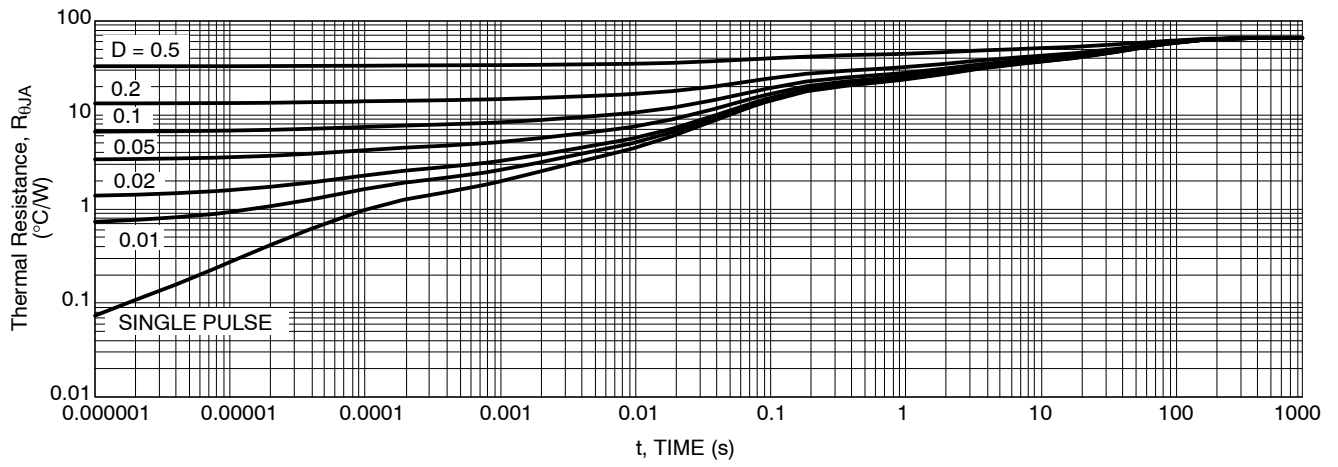


Figure 12. Thermal Response



TYPICAL CHARACTERISTICS – Q2

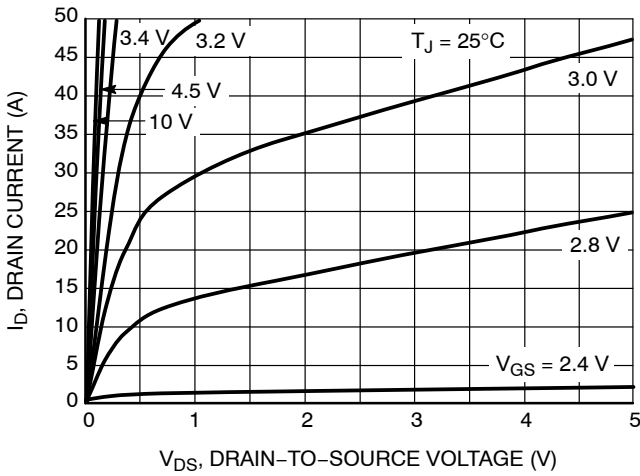


Figure 13. On-Region Characteristics

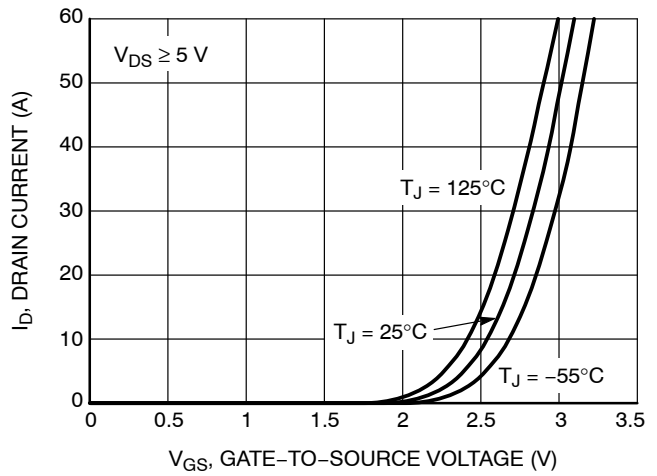


Figure 14. Transfer Characteristics

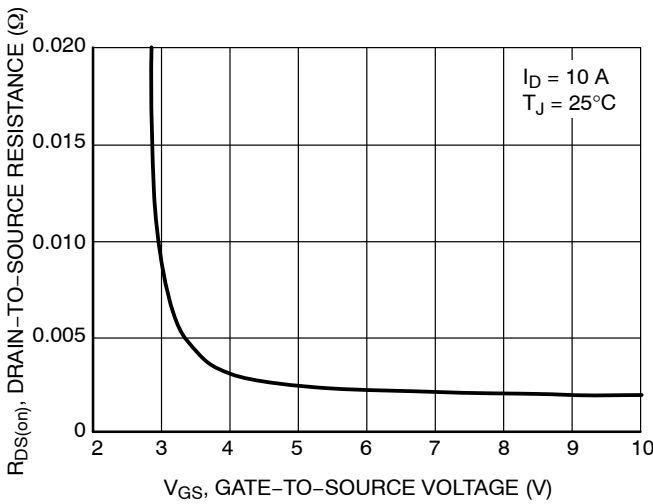


Figure 15. On-Resistance vs. Gate-to-Source Resistance

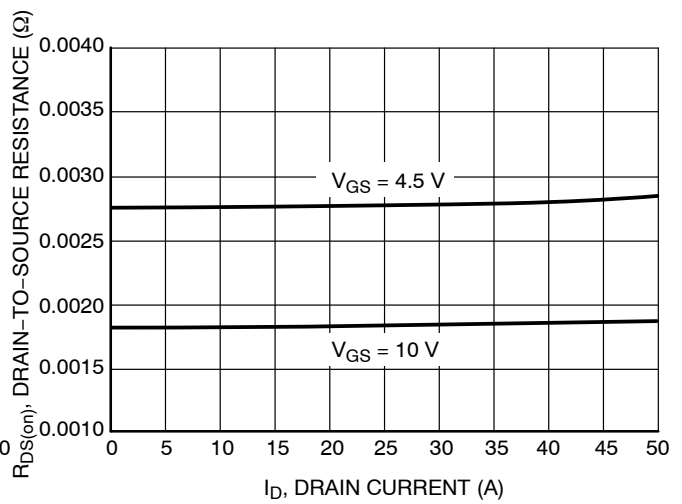


Figure 16. On-Resistance vs. Drain Current and Gate Voltage

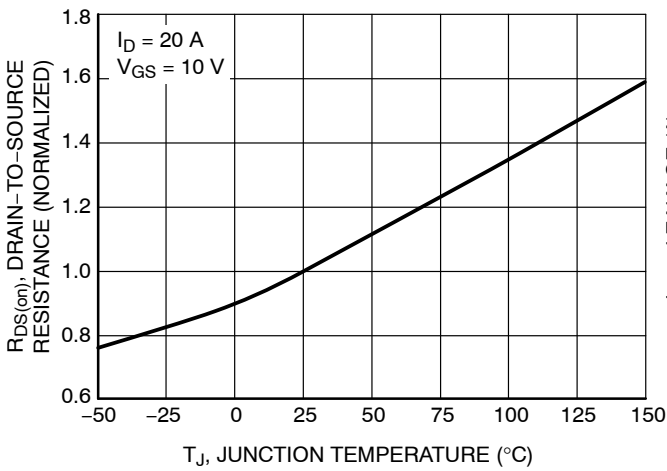


Figure 17. On-Resistance Variation with Temperature

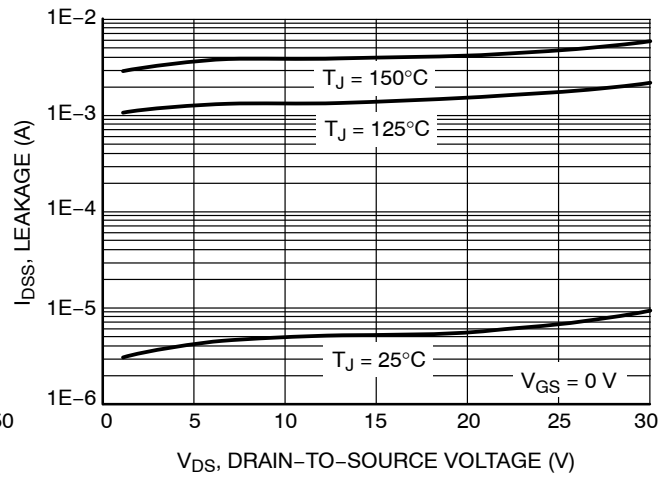
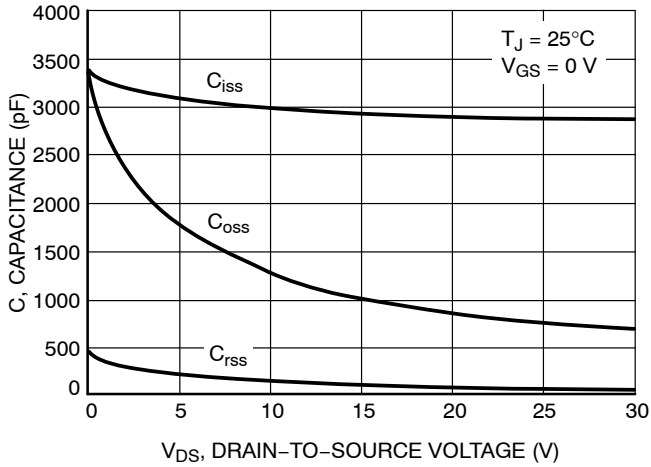


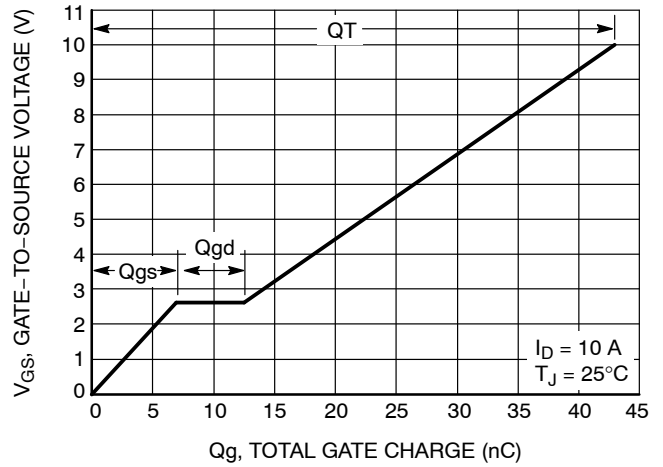
Figure 18. Drain-to-Source Leakage Current vs. Voltage

# NTMFD4901NF

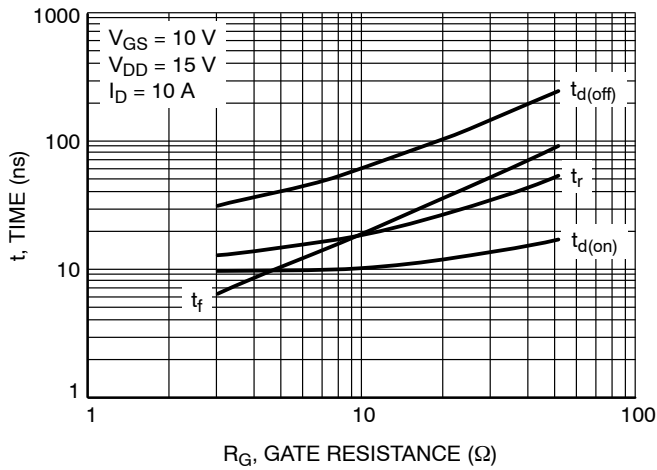
## TYPICAL CHARACTERISTICS – Q2



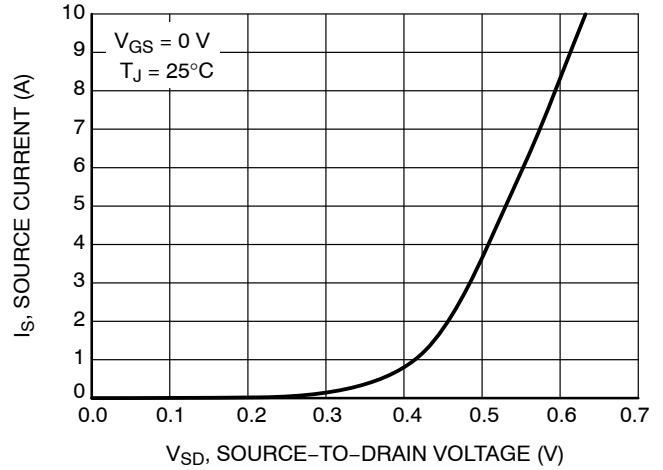
**Figure 19. Capacitance Variation**



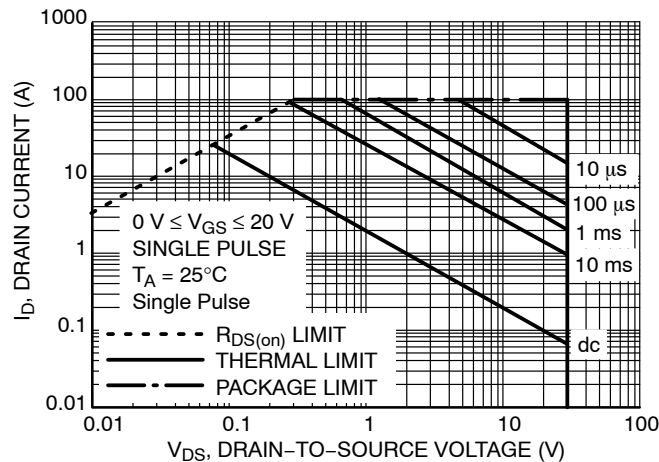
**Figure 20. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 21. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 22. Diode Forward Voltage vs. Current**



**Figure 23. Maximum Rated Forward Biased Safe Operating Area**

# NTMFD4901NF

## TYPICAL CHARACTERISTICS – Q2

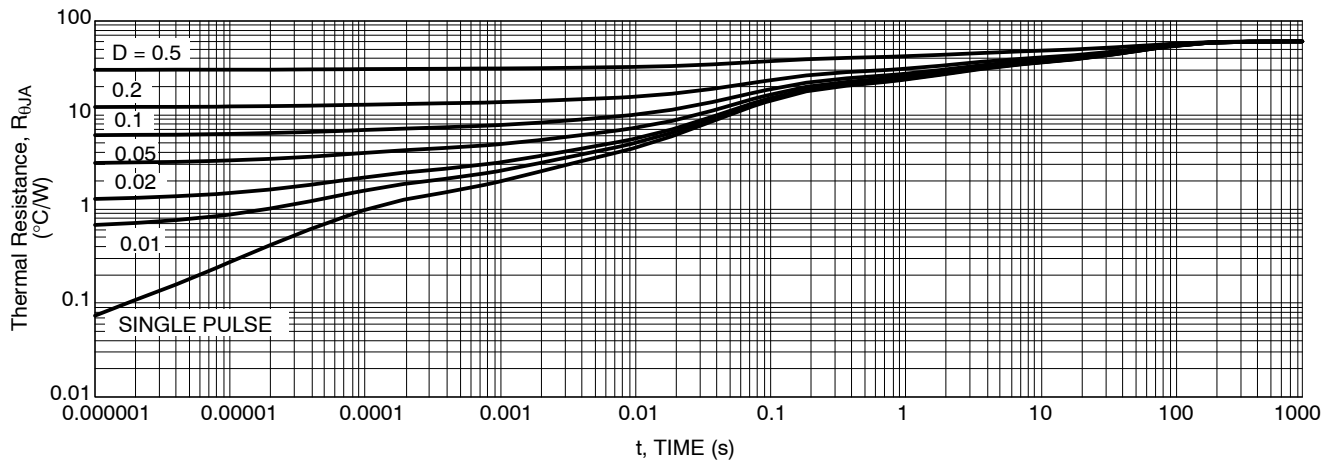
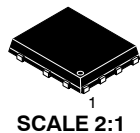


Figure 24. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

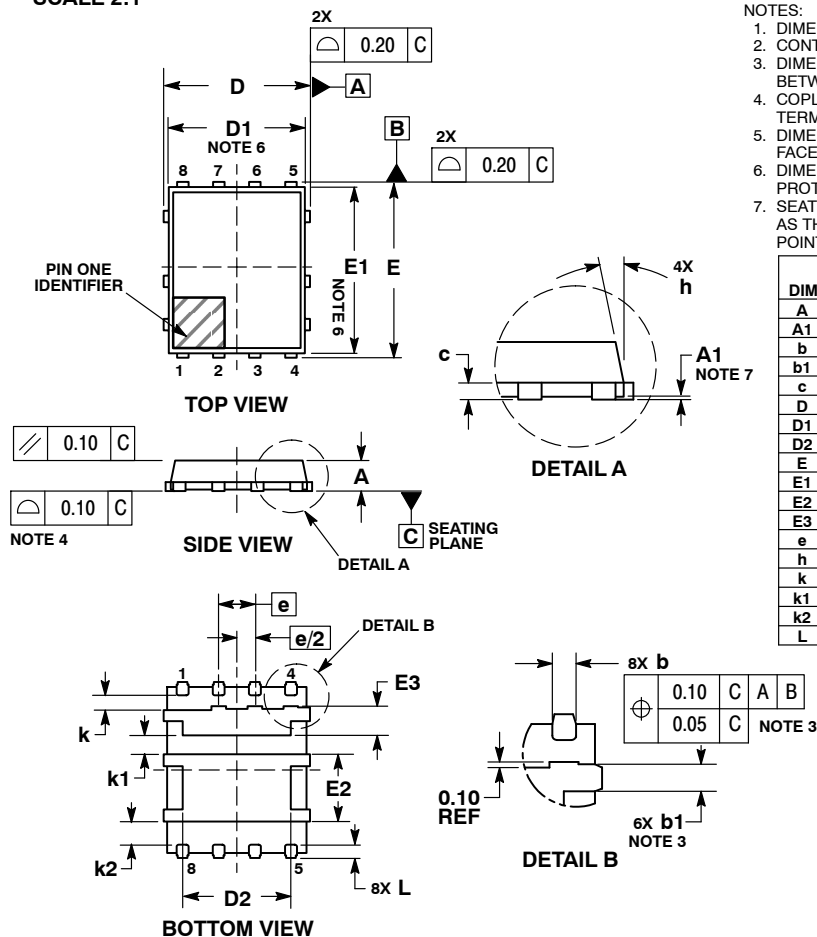
ON Semiconductor®



### DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual-Asymmetrical)

CASE 506BX  
ISSUE D

DATE 24 JUN 2014



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS b AND L ARE MEASURED AT THE PACKAGE SURFACE.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
7. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

MILLIMETERS		
DIM	MIN	MAX
A	0.90	1.10
A1	0.00	0.05
b	0.41	0.61
b1	0.41	0.61
c	0.23	0.33
D	5.00	5.30
D1	4.50	5.10
D2	3.50	4.22
E	6.00	6.30
E1	5.50	6.10
E2	2.27	2.67
E3	0.82	1.22
e	1.27 BSC	
h	---	12 °
k	0.39	0.59
k1	0.56	0.76
k2	0.73	0.93
L	0.35	0.55

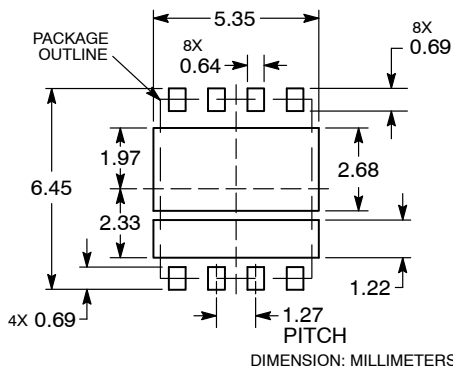
### GENERIC MARKING DIAGRAM\*



XXXXXX= Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking.

### RECOMMENDED SOLDERING FOOTPRINT\*



STYLE 1:

- PIN 1. GATE 1
- 2. DRAIN 1
- 3. DRAIN 1
- 4. DRAIN 1
- 5. SOURCE 2
- 6. SOURCE 2
- 7. SOURCE 2
- 8. GATE 2
- 9. DRAIN 1
- 10. SOURCE 1/DRAIN 2

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON54291E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL-ASYMMETRICAL)</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative