

NTMD6601NR2G

Power MOSFET

80 V, 2.2 A, Dual N-Channel, SO-8

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Dual SO-8 Surface Mount Package Saves Board Space
- This is a Pb-Free Device

Applications

- LCD Displays

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	80	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 15	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Continuous Drain Current $R_{\theta JA}$ $t < 5$ s (Note 1)	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	A
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	1.3	A
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^\circ\text{C}$, $V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 7.0$ A _{pk} , $L = 1.0$ mH, $R_G = 25 \Omega$	EAS	25	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	120	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5$ s (Note 1)	$R_{\theta JA}$	48	
Junction-to-FOOT (Drain)	$R_{\theta JF}$	40	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	200	

1. Surface-mounted on 2 inch sq FR4 board using 1 inch sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

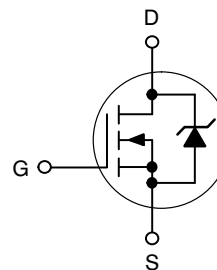


ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
80 V	215 m Ω @ 10 V	2.2 A
	245 m Ω @ 4.5 V	

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



6601N = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTMD6601NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMD6601NR2G

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			99.8		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V			1.0	μA
		T _J = 25°C				
		T _J = 125°C			25	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±15 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.9	3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			4.6		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 2.2 A		190	215	mΩ
		V _{GS} = 5.0 V, I _D = 1.0 A		215	245	

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		220	400	pF
Output Capacitance	C _{OSS}			55	100	
Reverse Transfer Capacitance	C _{RSS}			16	30	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 5.0 V, V _{DS} = 40 V, I _D = 1.0 A		5.0	9.0	nC
Threshold Gate Charge	Q _{G(TH)}			0.4		
Gate-to-Source Charge	Q _{GS}			1.0		
Gate-to-Drain Charge	Q _{GD}			2.75		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 40 V, I _D = 1.0 A		9.0	15	nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DD} = 40 V, I _D = 1.0 A, R _G = 27 Ω		21	35	ns
Rise Time	t _r			62	105	
Turn-Off Delay Time	t _{d(OFF)}			52	85	
Fall Time	t _f			50	85	
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DD} = 40 V, I _D = 2.5 A, R _G = 47 Ω		15		ns
Rise Time	t _r			95		
Turn-Off Delay Time	t _{d(OFF)}			50		
Fall Time	t _f			105		

BODY - DRAIN DIODE RATINGS (Note 3)

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _D = 1.0 A	T _J = 25°C		0.8	1.0	V
			T _J = 150°C		0.6		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dI _T = 100 A/μs, I _S = 1.0 A			44		ns
Charge Time	T _a				21		
Discharge Time	T _b				23		
Reverse Recovery Time	Q _{RR}				43	86	

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

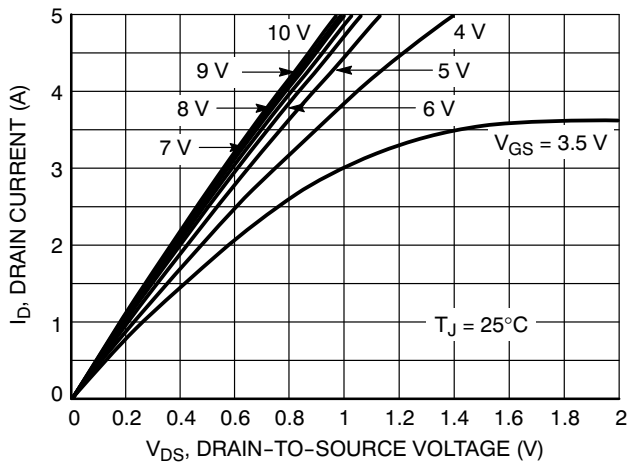


Figure 1. On-Region Characteristics

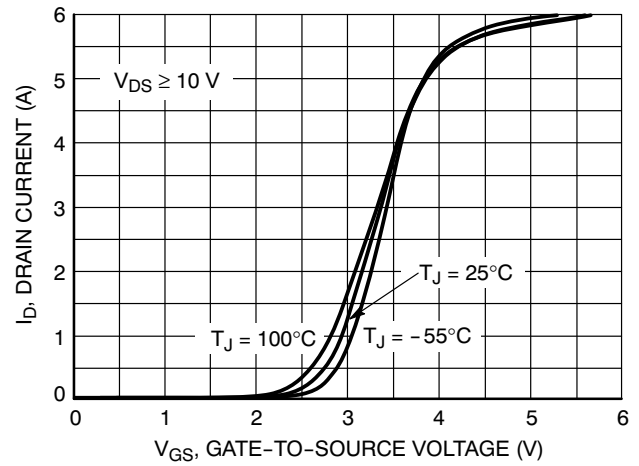


Figure 2. Transfer Characteristics

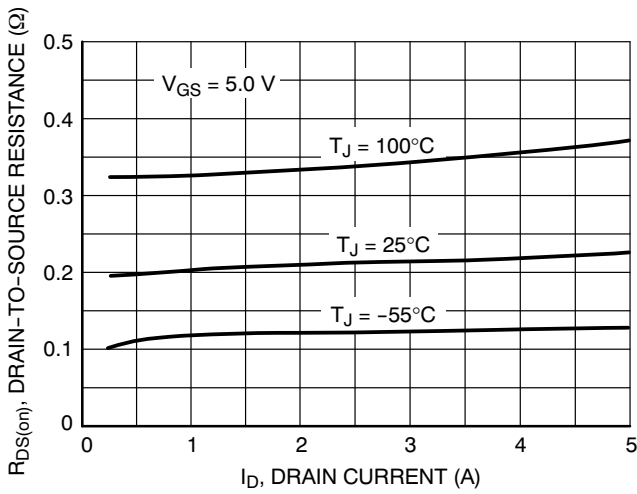


Figure 3. On-Resistance versus Drain Current and Temperature

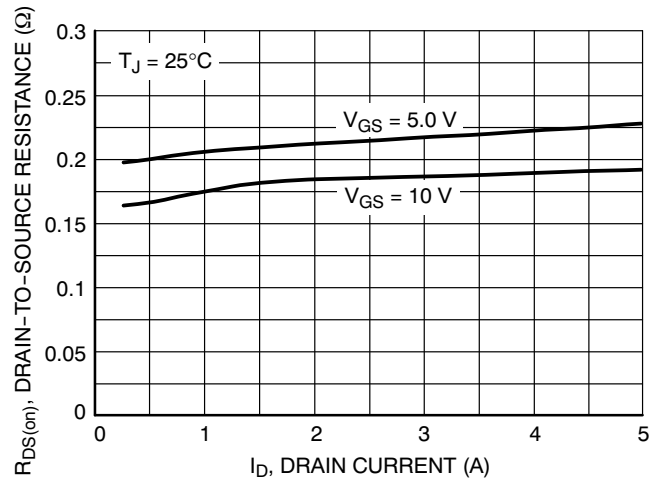


Figure 4. On-Resistance versus Drain Current and Gate Voltage

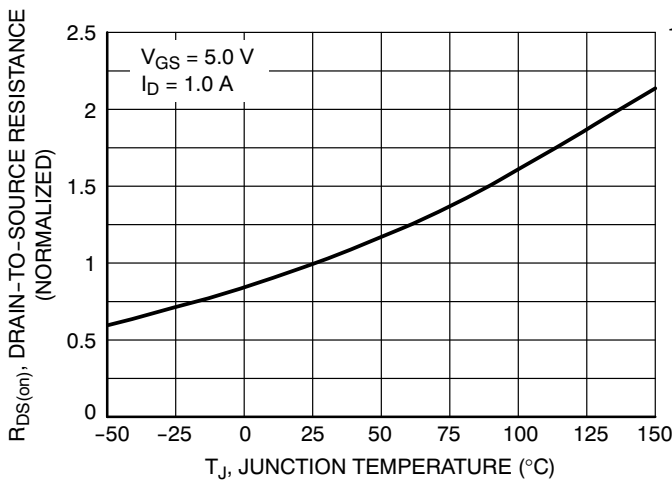


Figure 5. On-Resistance Variation with Temperature

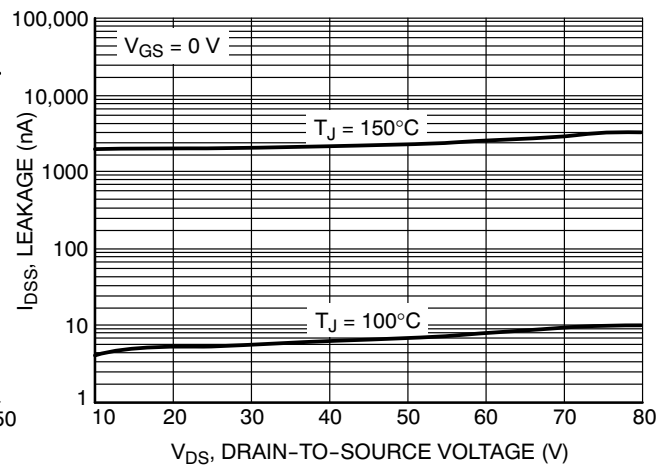


Figure 6. Drain-To-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

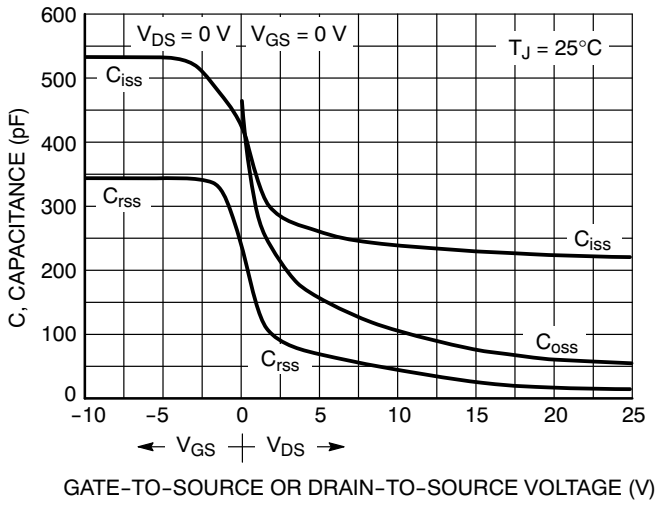


Figure 7. Capacitance Variation

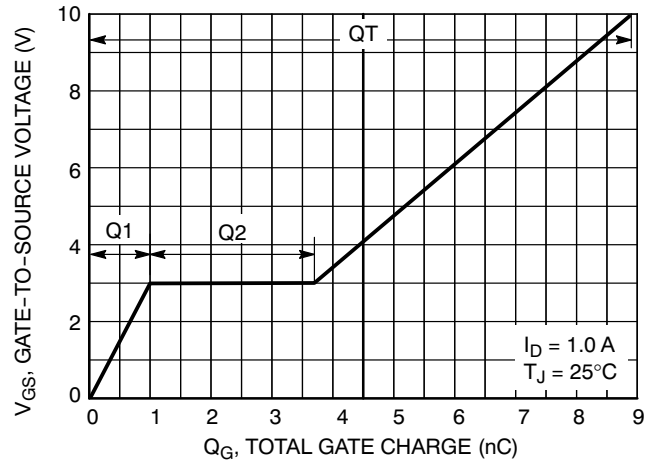


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

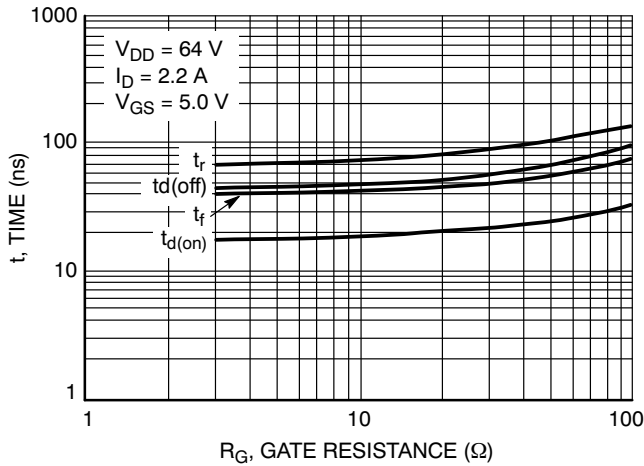


Figure 9. Resistive Switching Time Variation versus Gate Resistance

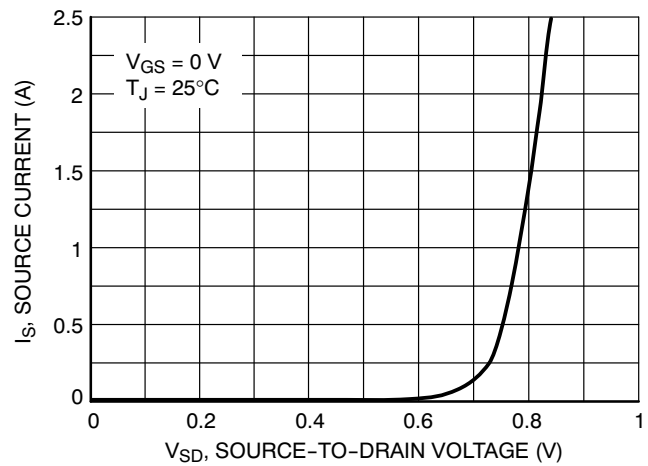


Figure 10. Diode Forward Voltage versus Current

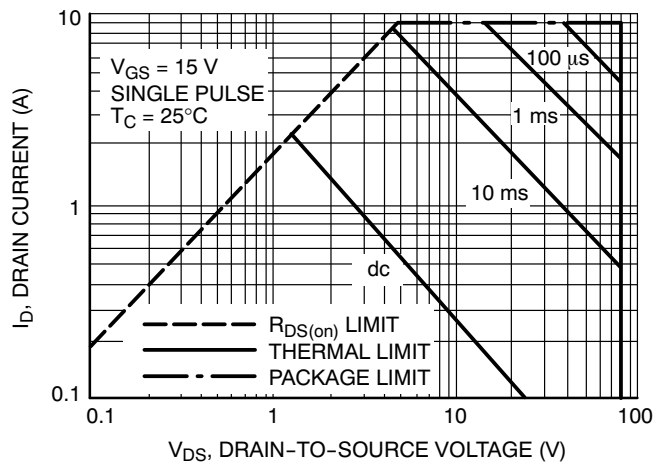


Figure 11. Maximum Rated Forward Biased Safe Operating Area

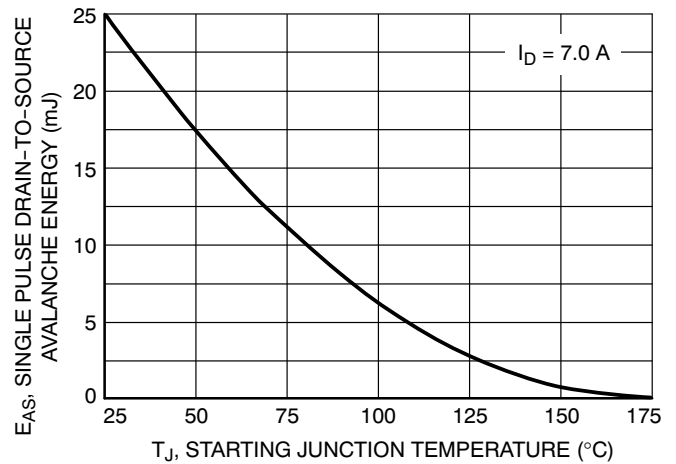


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

NTMD6601NR2G

TYPICAL ELECTRICAL CHARACTERISTICS

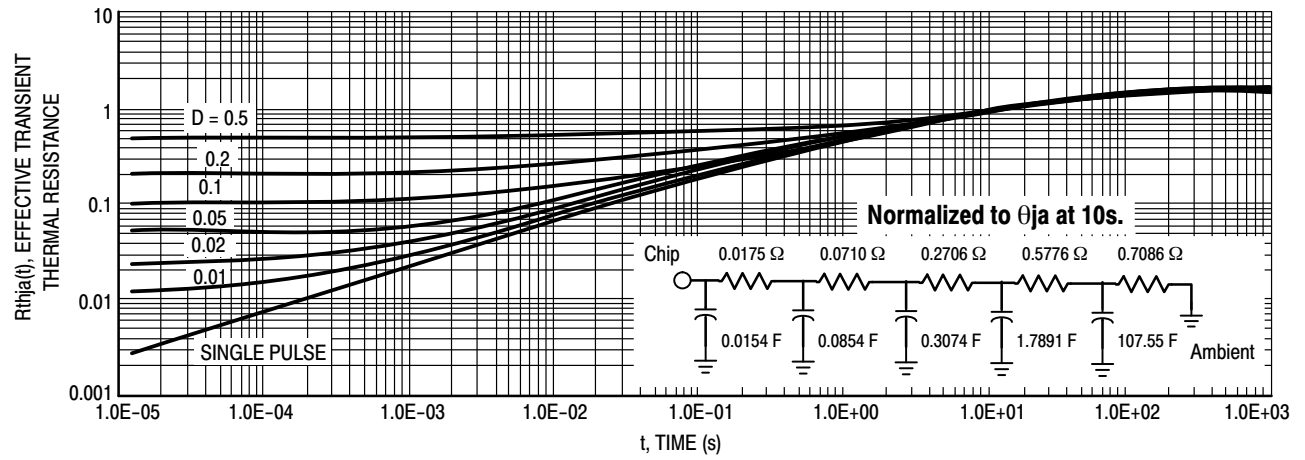


Figure 13. Thermal Response

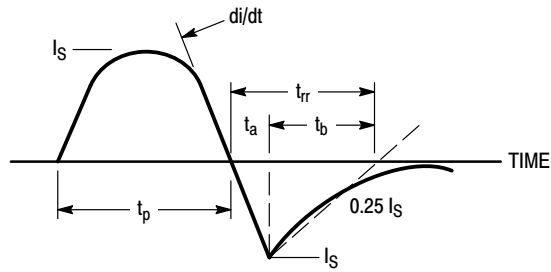
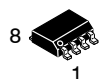


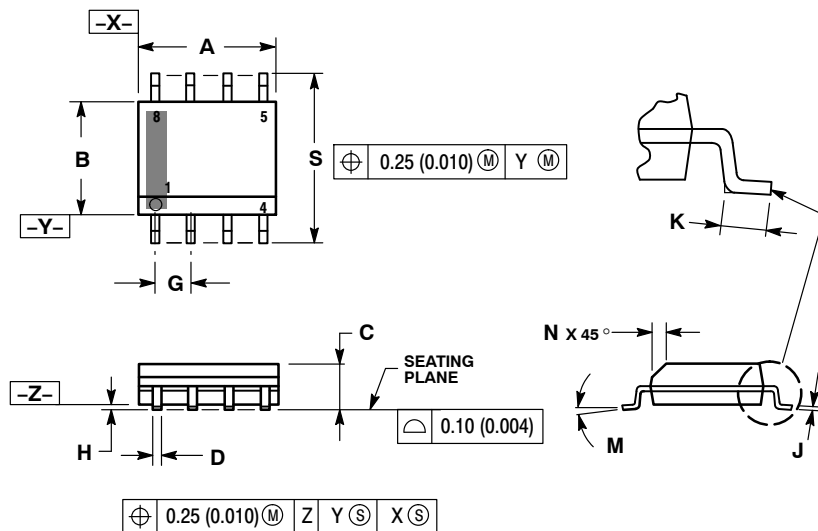
Figure 14. Diode Reverse Recovery Waveform



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

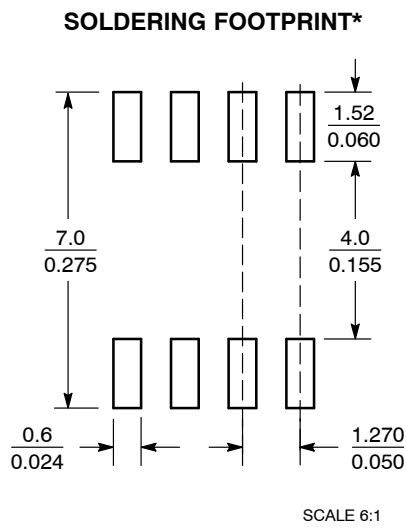


NOTES:

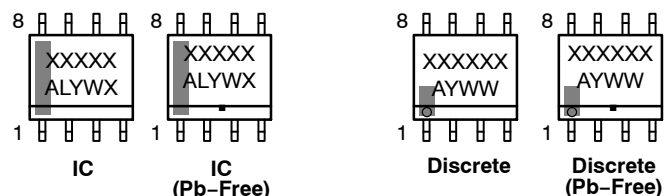
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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