NTLUD3A50PZ

MOSFET – Power, Dual, P-Channel, μCool, UDFN, 2.0x2.0x0.55 mm

-20 V, -5.6 A

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low $R_{DS(on)}$
- Low Profile UDFN 2.0x2.0x0.55 mm for Board Space Saving
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Side Load Switch
- Reverse Current Protection
- Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−4.4	A
		T_A = 85°C		−3.2	
	t ≤ 5 s	T_A = 25°C		−5.6	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.4	W
	t ≤ 5 s	T_A = 25°C		2.2	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−2.8	A
		T_A = 85°C		−2.0	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.5	W
Pulsed Drain Current		tp = 10 μs	I_{DM}	−13	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	°C
ESD (HBM, JESD22−A114) (MM, JESD22−A114)			V_{ESD}	1400 200	V
Source Current (Body Diode) (Note 2)			I_S	−1.0	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.

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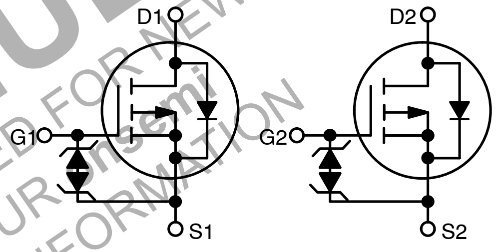
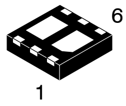
MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−20 V	50 mΩ @ −4.5 V	−5.6 A
	70 mΩ @ −2.5 V	
	115 mΩ @ −1.8 V	
	175 mΩ @ −1.5 V	

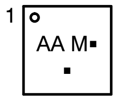


P−Channel MOSFET

MARKING DIAGRAM

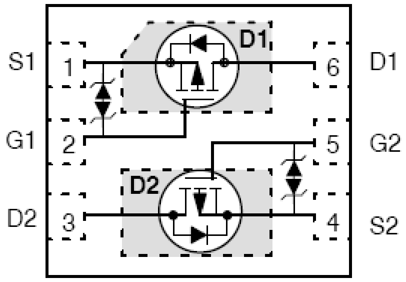


UDFN6
CASE 517BF
μCOOL™



AA = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

May, 2024 − Rev. 3

2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm^2, 1 oz. Cu based on both FETs on.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	91	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 3)	$R_{\theta JA}$	57	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	228	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			−13		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −20 V	T_J = 25°C			−1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5.0 V				±5.0	μA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.4		−1.0	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$				3.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −4.0 A			37	50	mΩ
		V_{GS} = −2.5 V, I_D = −3.0 A			46	70	
		V_{GS} = −1.8 V, I_D = −2.0 A			63	115	
		V_{GS} = −1.5 V, I_D = −1.0 A			86	175	
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V, I_D = −3.0 A			16		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = −15 V			920		pF
Output Capacitance	C_{OSS}				85		
Reverse Transfer Capacitance	C_{RSS}				80		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V; I_D = −3.0 A			10.4		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.5		
Gate-to-Source Charge	Q_{GS}				1.2		
Gate-to-Drain Charge	Q_{GD}				3.0		
SWITCHING CHARACTERISTICS, VGS = 4.5 V (Note 6)							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −3.0 A, R_G = 1 Ω			7.0		ns
Rise Time	t_r				12		
Turn-Off Delay Time	$t_{d(OFF)}$				39		
Fall Time	t_f				30		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	VSD	V_{GS} = 0 V, I_S = −1.0 A	T_J = 25°C		−0.67	−1.0	V
			T_J = 125°C		−0.56		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.
4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm^2, 1 oz. Cu based on both FETs on.
5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dis/dt = 100 A/μs, I_S = −1.0 A		12.1		ns
Charge Time	t_a			6.4		
Discharge Time	t_b			5.7		
Reverse Recovery Charge	Q_{RR}			4.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.
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5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
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TYPICAL CHARACTERISTICS

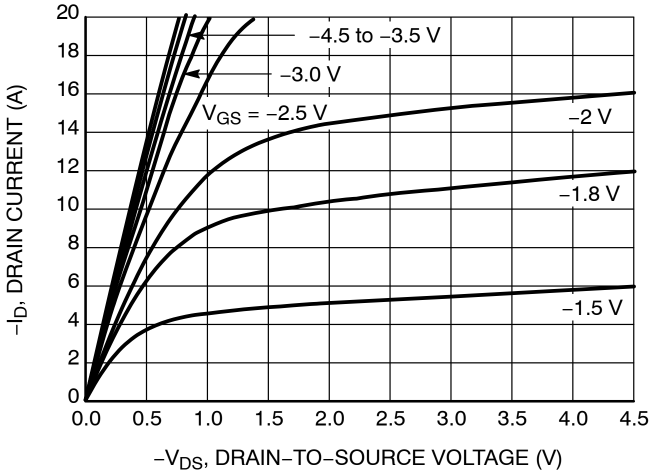


Figure 1. On−Region Characteristics

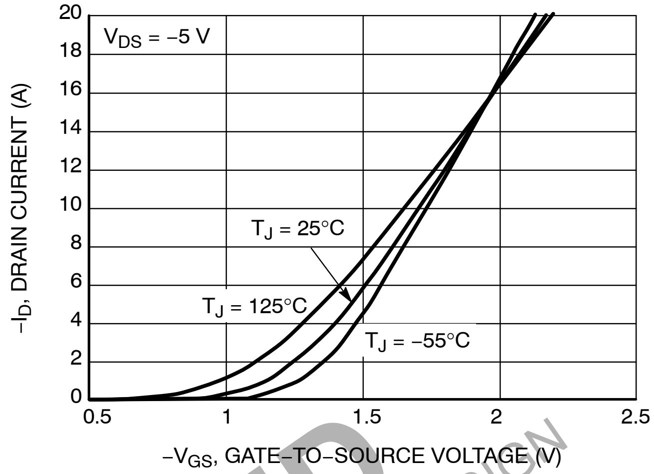


Figure 2. Transfer Characteristics

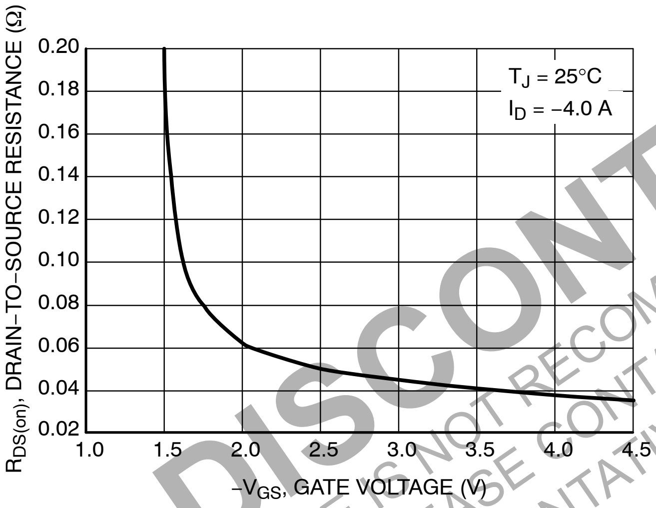


Figure 3. On−Resistance vs. Gate−to−Source Voltage

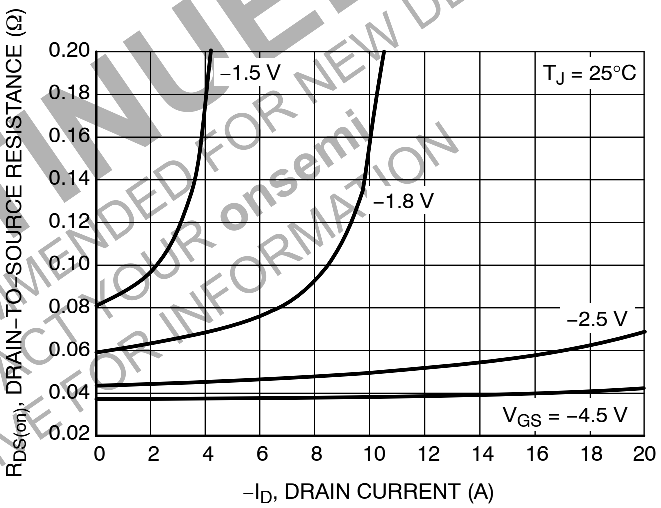


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

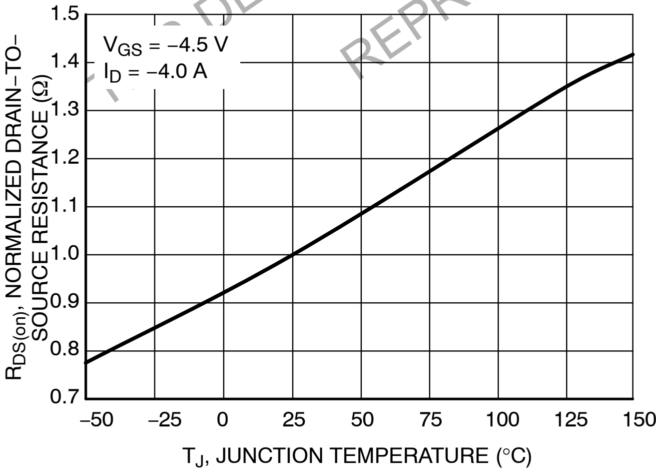


Figure 5. On−Resistance Variation with Temperature

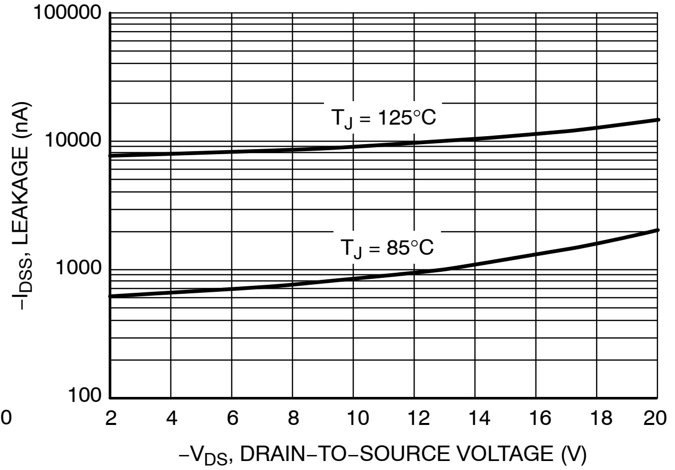


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

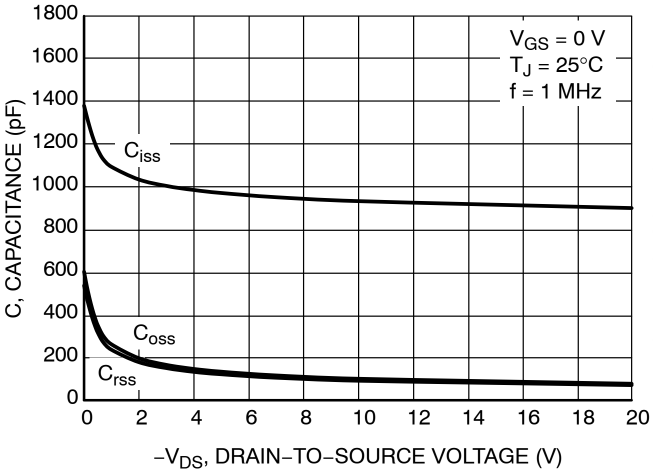


Figure 7. Capacitance Variation

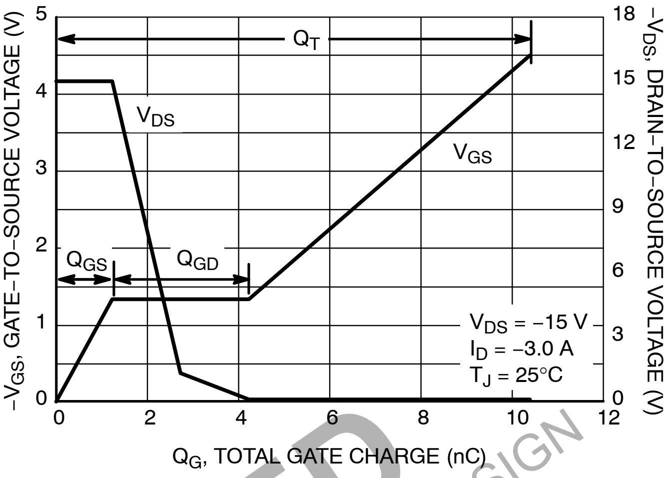


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

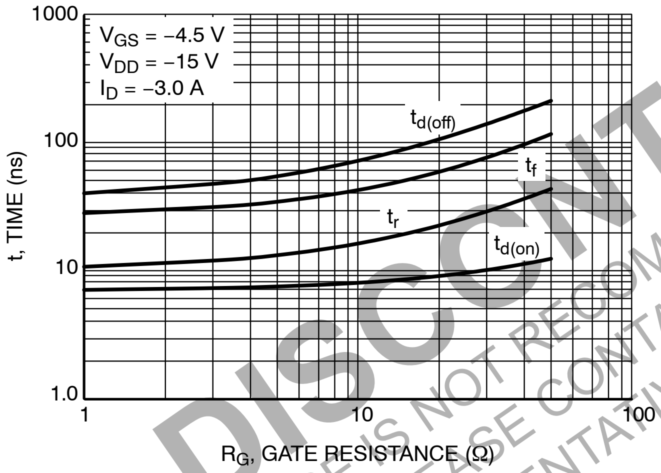


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

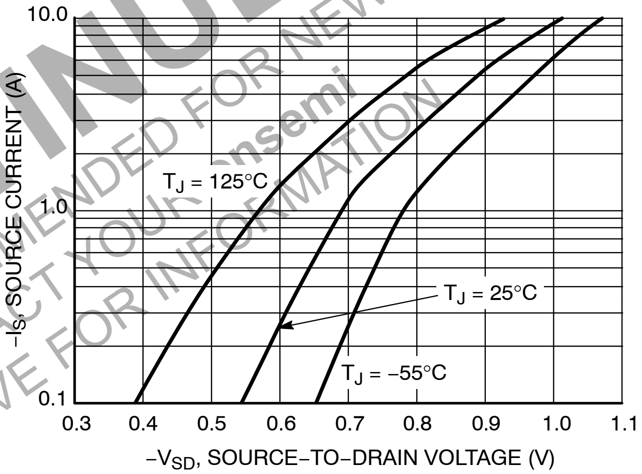


Figure 10. Diode Forward Voltage vs. Current

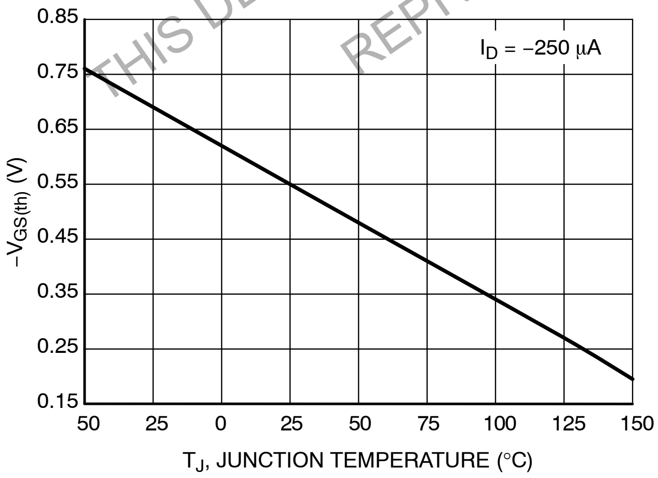


Figure 11. Threshold Voltage

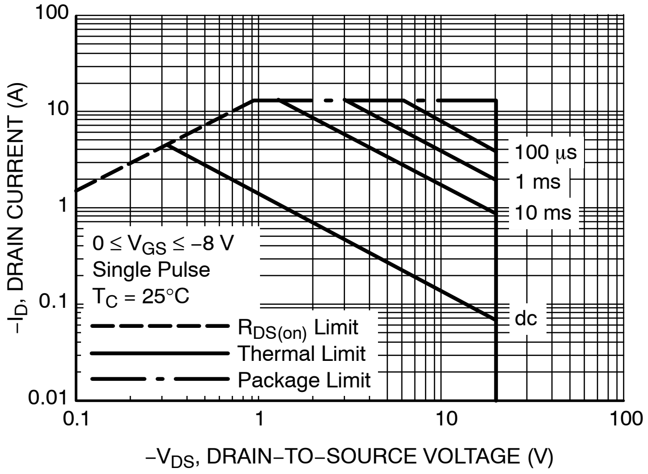


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

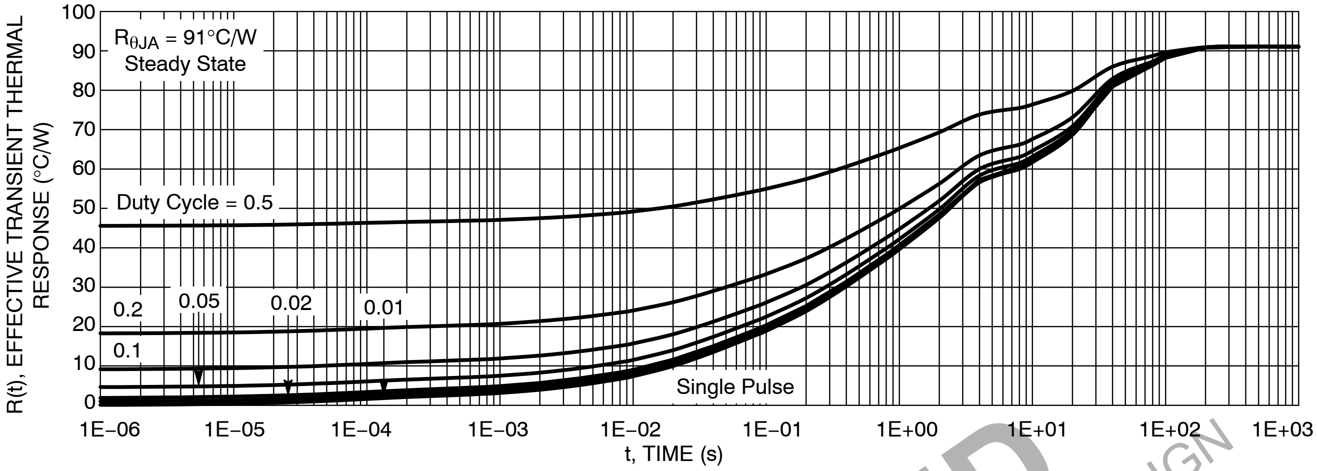
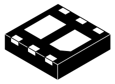


Figure 13. FET Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTLUD3A50PZTAG	UDFN6 (Pb−Free)	3000 / Tape & Reel
NTLUD3A50PZTBG	UDFN6 (Pb−Free)	3000 / Tape & Reel

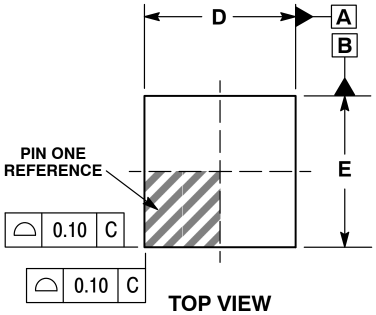
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



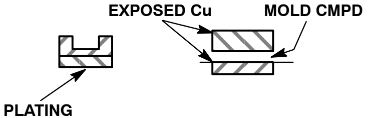
SCALE 4:1

UDFN6 2x2, 0.65P
CASE 517BF
ISSUE B

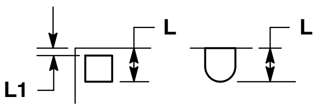
DATE 20 AUG 2012



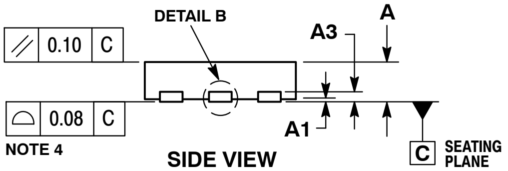
TOP VIEW



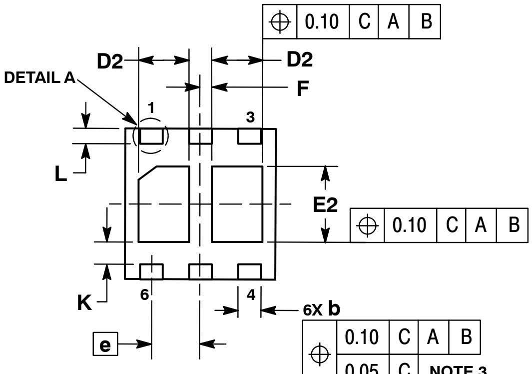
DETAIL B
OPTIONAL CONSTRUCTIONS



DETAIL A
OPTIONAL CONSTRUCTIONS



SIDE VIEW

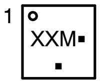


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.15 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10

GENERIC MARKING DIAGRAM*

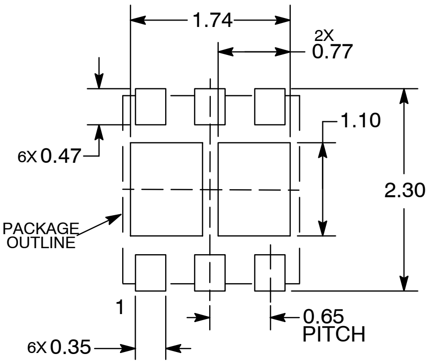


XX = Specific Device Code
M = Date Code

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**UDFN6 2x2, 0.65P**	**PAGE 1 OF 1**

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