

# NTLTS3107P

## Power MOSFET

-20 V, -8.3 A, Single P-Channel,  
Micro8 Leadless Package

### Features

- Low  $R_{DS(on)}$  for Extended Battery Life
- Surface Mount Micro8 Leadless for Improved Thermal Performance
- Low Profile (<1.0 mm) Optimal for Portable Designs
- Low Turn-On Voltage
- This is a Pb-Free Device

### Applications

- Optimized for Load Management Applications
- Charge Control in Battery Powered Systems
- Cell Phones, DSC, Notebooks, Portable Games, etc.

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	-20	V
Gate-to-Source Voltage			V <sub>GS</sub>	± 8.0	V
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	-8.3	A
		T <sub>A</sub> = 85°C		-6.0	
	t ≤ 10 s	T <sub>A</sub> = 25°C		-12	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.6	W
	t ≤ 10 s			3.3	
Continuous Drain Current (Note 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	-5.9	A
		T <sub>A</sub> = 85°C		-3.7	
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.8	W
Pulsed Drain Current (Note 1)	t <sub>p</sub> = 10 μs		I <sub>DM</sub>	-25	A
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
Source Current (Body Diode)			I <sub>S</sub>	-1.6	A
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			T <sub>L</sub>	260	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	38	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	160	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq. in. pad size (Cu. area = 1.127 sq. in. [1 oz] including traces).
2. Surface-mounted on FR4 board using minimum recommended pad size (Cu. area = TBD sq. in.).

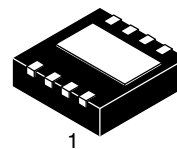
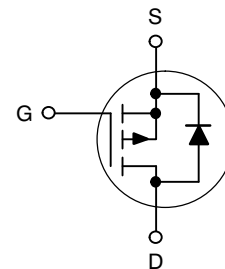


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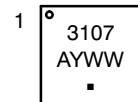
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-20 V	12.2 m $\Omega$ @ -4.5 V	-8.3 A
	15.6 m $\Omega$ @ -2.5 V	
	26.2 m $\Omega$ @ -1.8 V	

### P-Channel MOSFET



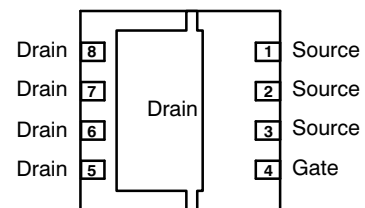
Micro8 Leadless  
CASE 846C

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

### PIN ASSIGNMENT



(Bottom View)

### ORDERING INFORMATION

Device	Package	Shipping†
NTLTS3107PR2G	Micro8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTLTS3107P

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			11		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V			-10	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8.0 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-0.45		-1.2	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			3.4		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -8.0 A		12.2	16	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -7.0 A		15.6	21	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -5.8 A		26.2		
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -8.0 A		25		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = -16 V		5900	6500	pF
Output Capacitance	C <sub>OSS</sub>			625	675	
Reverse Transfer Capacitance	C <sub>RSS</sub>			425	525	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -16 V, I <sub>D</sub> = -8.0 A		55	70	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			3.0		
Gate-to-Source Gate Charge	Q <sub>GS</sub>			7.0		
Gate-to-Drain "Miller" Charge	Q <sub>GD</sub>			11		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -8.0 A, R <sub>G</sub> = 3.0 Ω		30		ns
Rise Time	t <sub>r</sub>			20		
Turn-Off Delay Time	t <sub>d(off)</sub>			250		
Fall Time	t <sub>f</sub>			80		

### DRAIN-SOURCE DIODE CHARACTERISTICS (Note 3)

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.6 A	T <sub>J</sub> = 25°C		-0.7	-1.2	V
			T <sub>J</sub> = 125°C		0.5		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = -1.6 A			75	100	ns
Charge Time	t <sub>a</sub>				28		
Discharge Time	t <sub>b</sub>				47		
Reverse Recovery Charge	Q <sub>RR</sub>				81.5		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

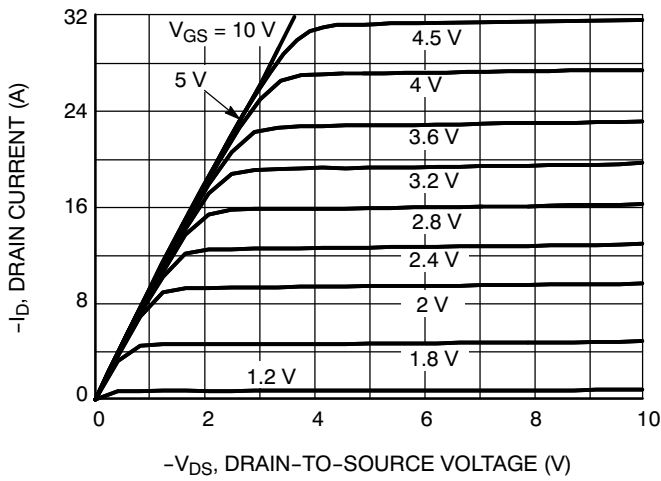


Figure 1. On-Region Characteristics

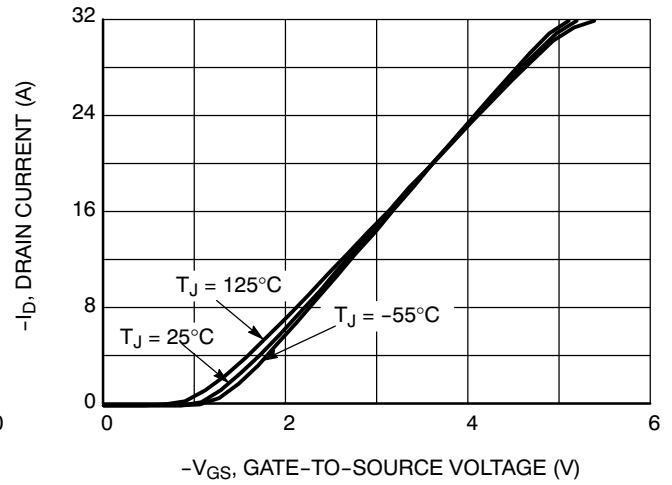


Figure 2. Transfer Characteristics

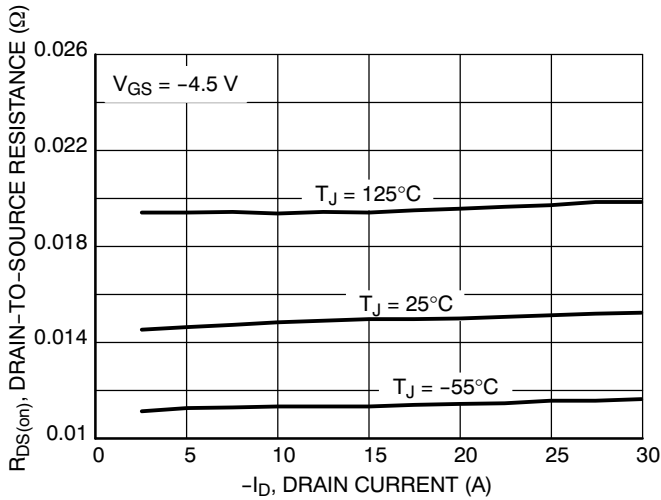


Figure 3. On-Resistance versus Drain Current and Temperature

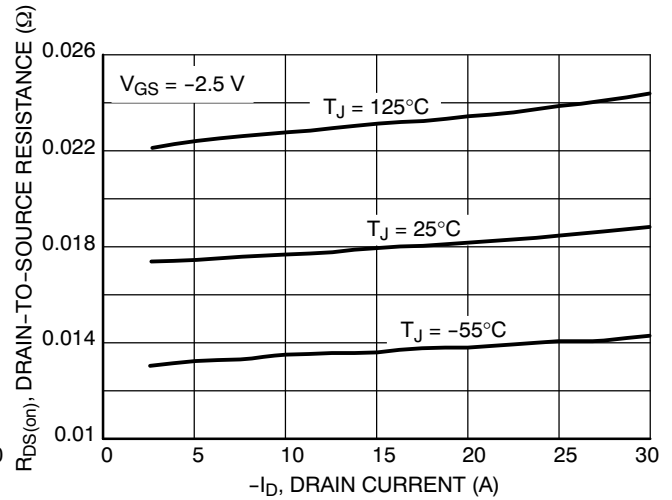


Figure 4. On-Resistance versus Drain Current and Temperature

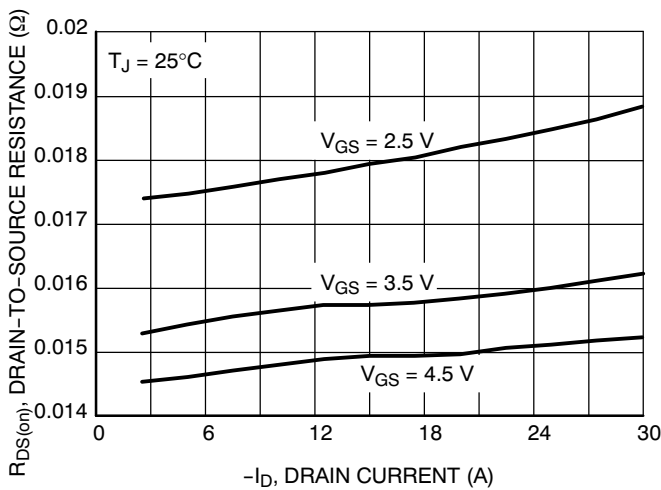


Figure 5. On-Resistance versus Drain Current and Gate Voltage

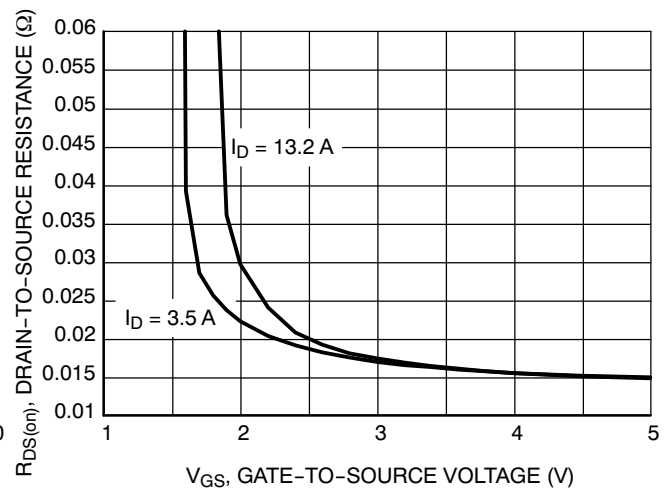
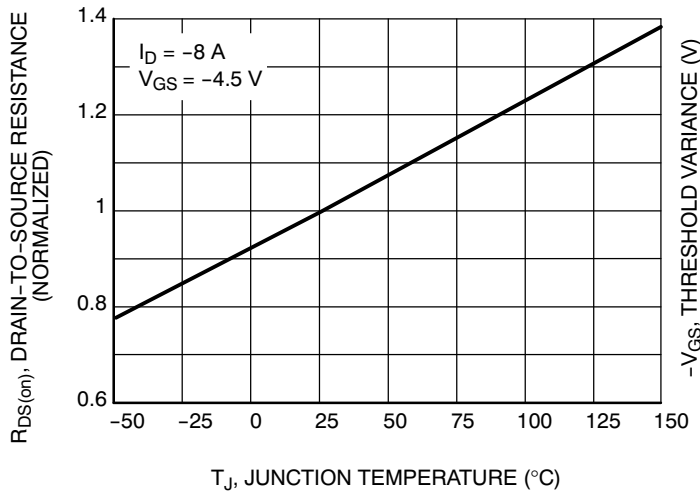
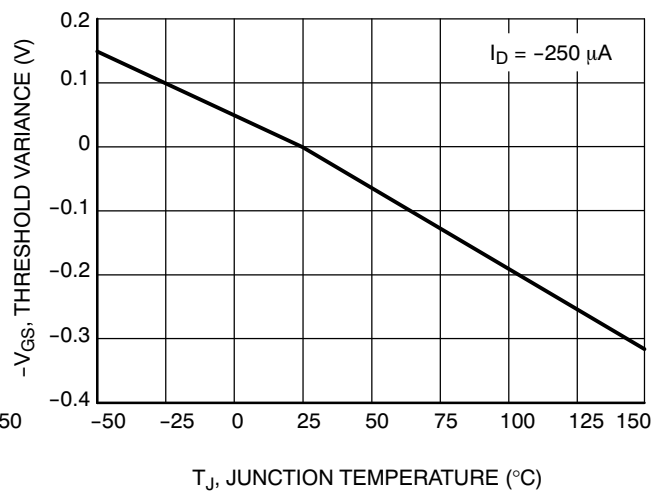


Figure 6. On-Resistance versus Gate Voltage

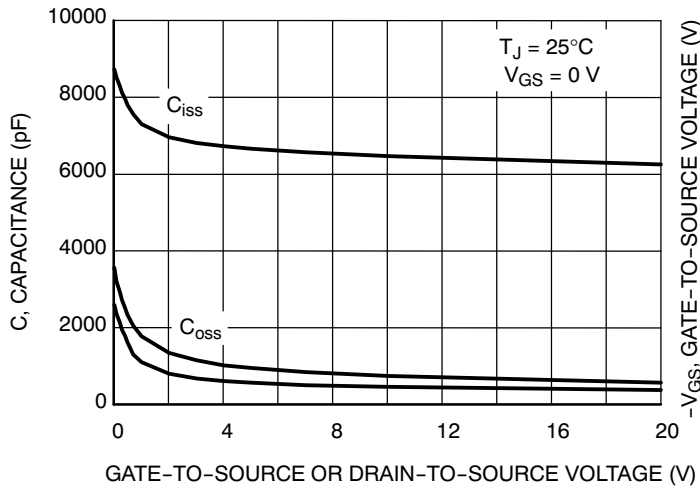
# NTLTS3107P



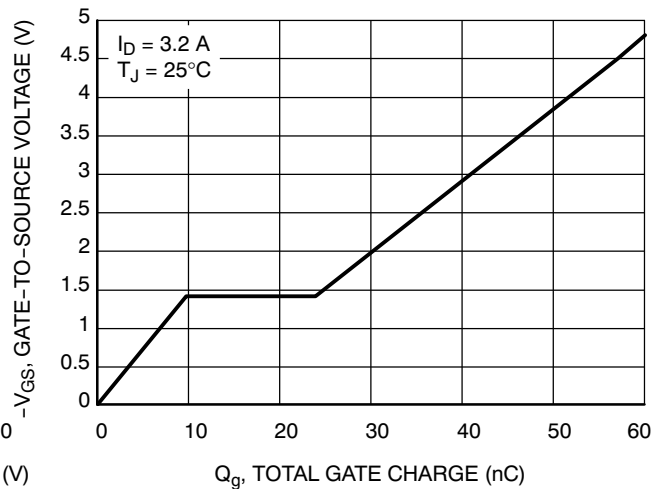
**Figure 7. On-Resistance Variation with Temperature**



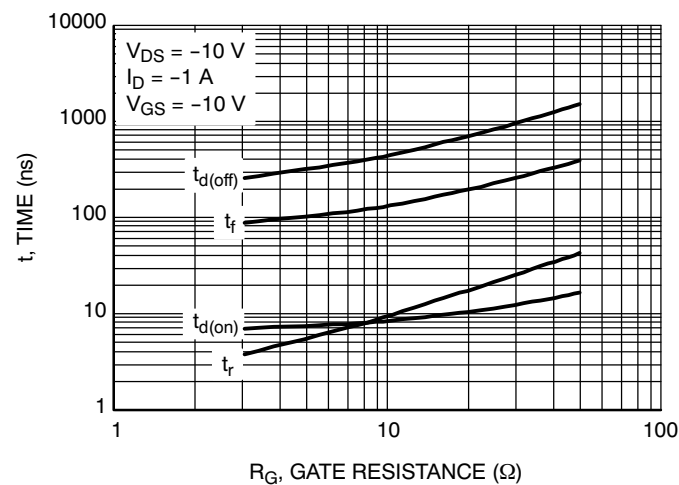
**Figure 8. Threshold Voltage**



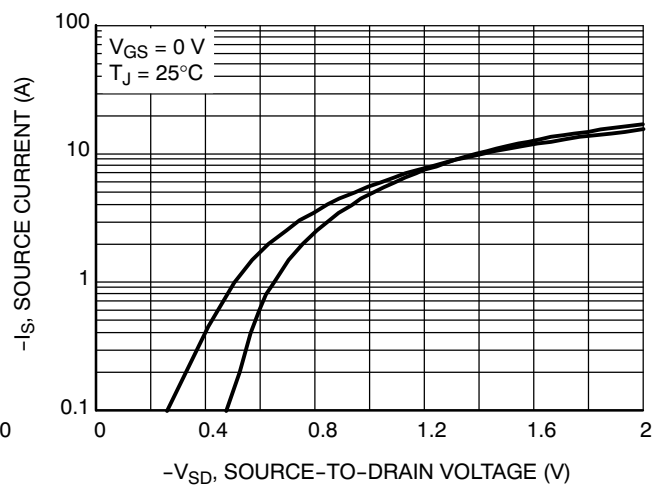
**Figure 9. Capacitance Variation**



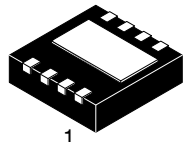
**Figure 10. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



**Figure 11. Resistive Switching Time Variation versus Gate Resistance**

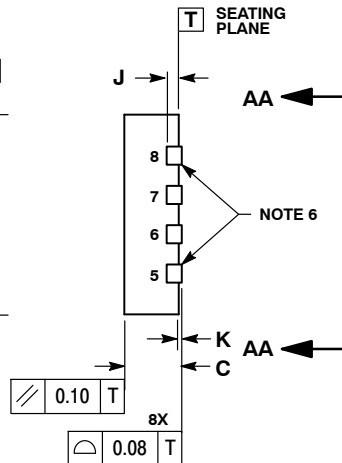
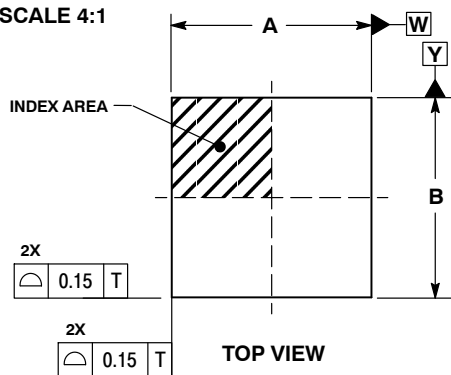


**Figure 12. Diode Forward Voltage versus Current**


**DFN8 3x3, (MICRO8 LEADLESS)**  
CASE 846C-01  
ISSUE D

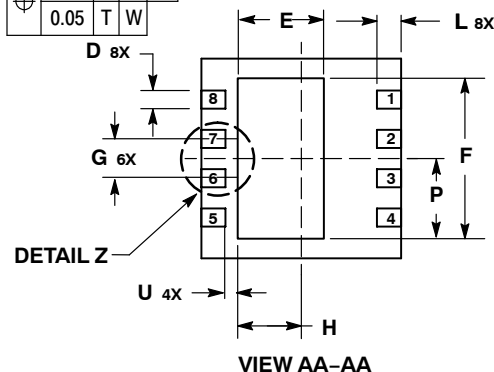
DATE 28 JUN 2010

SCALE 4:1

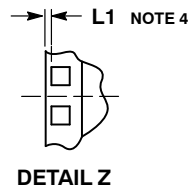


NOTE 4

⊕	0.10	T	W	Y
	0.05	T	W	



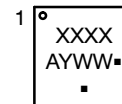
SIDE VIEW



## NOTES:

- DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETER.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION D APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 0.30 MM FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE, UP TO 0.1 MM IS ACCEPTABLE. L1 IS OPTIONAL.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- OPTIONAL SIDE VIEW CAN SHOW LEADS 5 AND 8 REMOVED.

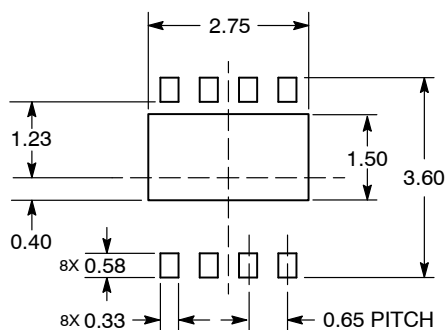
MILLIMETERS		
DIM	MIN	MAX
A	3.30	BSC
B	3.30	BSC
C	0.85	0.95
D	0.25	0.35
E	1.30	1.50
F	2.55	2.75
G	0.65	BSC
H	0.95	1.15
J	0.25	BSC
K	0.00	0.05
L	0.35	0.45
L1	0.00	0.10
P	1.28	1.38
U	0.17	TYP

**GENERIC MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***


DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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