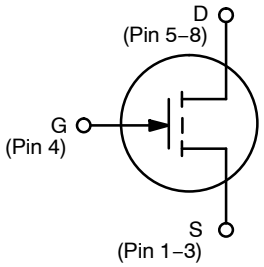
Enhancement Mode Gallium Nitride (GaN) HEMT

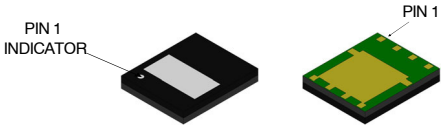
100 V, 1.9 mΩ, 275 A, PDSO-N8 5.0x6.0

Preliminary Document

NTLEF2D5N10GN1

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_{DS} MAX
100 V	1.9 mΩ	275 A





PDSO-N8 5.00x6.00x0.87, 1.27P
CASE 144AD

Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- FOM-Q_G = 20.9 nC*mΩ
- Small Footprint for High Density PCB Design
- Pb-Free, Halide Free and RoHS Compliant

Typical Applications

- High Density Power Modules
- High Frequency DC-DC Converters
- High Power Synchronous Rectifiers
- Motor Drivers

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	V
Drain-to-Source Transient Voltage, t_P < 100 μs	$V_{DS(TRAN)}$	120	V
Gate-to-Source Voltage	V_{GS}	−4 to 6	V
Gate-to-Source Transient Voltage, t_P = 100 ns, f_P = 100 kHz, open drain	$V_{GS(PULSE)}$	6.5	V
Continuous Drain Current, T_{CASE} = 25 °C T_{CASE} = 100 °C	I_{DS}	 275 174	A
Pulsed Drain Current, t_P < 100 μs, T_J = 25 °C T_J = 150 °C	$I_{DS(PULSE)}$	 540 420	A
Power Dissipation, V_{GS} = 5 V, T_{CASE} = 25 °C	P_{TOT}	378	W
Operating Junction Temperature	T_J	−55 to 150	°C
Storage Temperature	T_{STG}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

This Preliminary document is for informational purposes only. **onsemi** may update or withdraw it without notice. Content and referenced products are under development and subject to change.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction-to-Cases	$R_{\theta JC}$	0.3	°C/W
Junction-to-Board	$R_{\theta JB}$	3.6	°C/W
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	40	°C/W
Maximum Soldering Temperature (MSL3)	T_{SLD}	260	°C

1. Device on 1 in^2, 2 oz copper pad on single layer FR-4 PCB.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	100			V
Drain-to-Source Leakage Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V		1.4	TBD	μA
		V_{GS} = 0 V, V_{DS} = 100 V, T_J = 125 °C		300		
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 6 V, V_{DS} = 0 V		1.4	TBD	μA
		V_{GS} = 6 V, V_{DS} = 0 V, T_J = 125 °C		30		μA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 5 V, I_{DS} = 40 A		1.9	2.5	mΩ
		V_{GS} = 5 V, I_{DS} = 40 A, T_J = 125 °C		3.0		
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_{DS} = 10 mA, T_J = 25 °C		1.2		V
		V_{DS} = V_{GS}, I_{DS} = 10 mA, T_J = 125 °C		1.1		
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		1394		pF
Output Capacitance	C_{OSS}			566		
Reverse Transfer Capacitance	C_{RSS}			8.8		
Output Capacitance, Energy Related	$C_{OSS(ER)}$	V_{DS} = 0 V to 50 V, V_{GS} = 0 V		790		pF
Output Capacitance, Time Related	$C_{OSS(TR)}$			1119		
Output Charge	Q_{OSS}			56		nC
Output Capacitance Stored Energy	E_{OSS}			1.0		μJ
Gate Resistance	R_G	f = 5 MHz		0.7		Ω
Gate Charge	Q_G	V_{DS} = 50 V, I_{DS} = 40 A, V_{GS} = 0/5 V		11		nC
Gate-to-Source Charge	Q_{GS}			2.6		
Gate-to-Drain Charge	Q_{GD}			1.7		
Gate Plateau Voltage	V_{PLAT}			1.9		V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DS} = 50 V, I_{DS} = 40 A, V_{GS} = 0/5 V, R_G = 4 Ω		TBD		ns
Turn-Off Delay Time	$t_{D(OFF)}$			TBD		ns
Turn-On Rise Time	t_R			TBD		ns
Turn-Off Fall Time	t_F			TBD		ns
REVERSE CONDUCTION CHARACTERISTICS						
Source-to-Drain Reverse Voltage	V_{SD}	V_{GS} = −3 V, I_{SD} = 40 A		4.9		V
		V_{GS} = 0 V, I_{SD} = 40 A		1.9		
		V_{GS} = 5 V, I_{SD} = 40 A		0.08		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Share Feedback
Your Opinion Matters

GATE DRIVE GUIDELINES

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of **5 – 6 V** is recommended, with optional negative gate bias for hard-switching applications to improve dv/dt immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

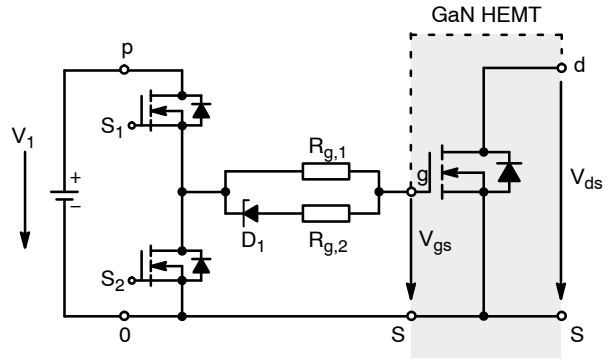


Figure 1. Schottky Gate Conventional Driver Schematic

ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
ENGNTLEF2D5N10GN1TXG	PDSO-N8 5.00x6.00x0.87, 1.27P	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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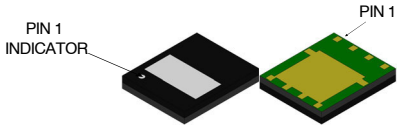
REVISION HISTORY

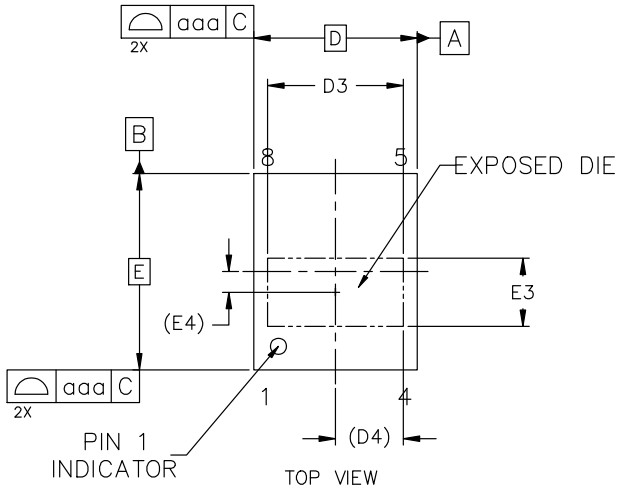
Revision	Description of Changes	Date
P0	Initial Preliminary document release.	4/3/2026
P1	Update – Package and Shipping information, Marking Diagram.	6/30/2026

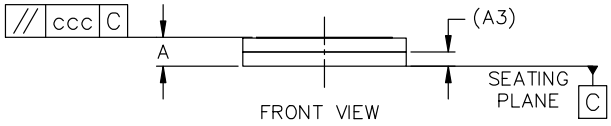
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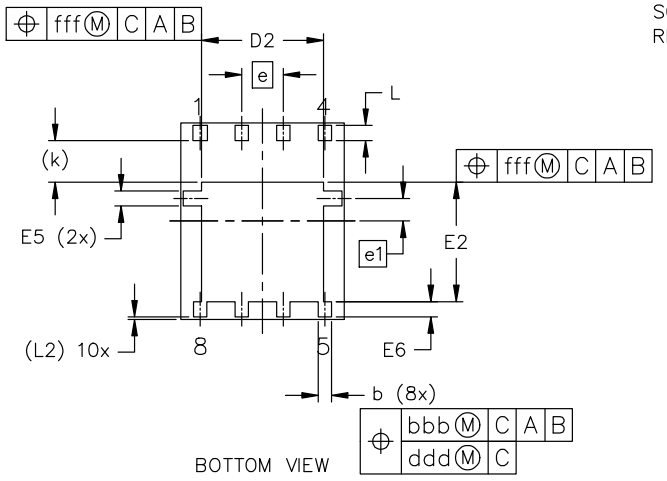
PDSO-N8 5.00x6.00x0.87, 1.27P
CASE 144AD
ISSUE A

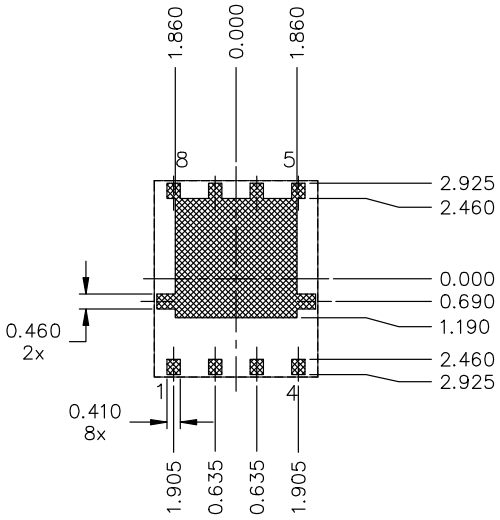
DATE 04 MAY 2026









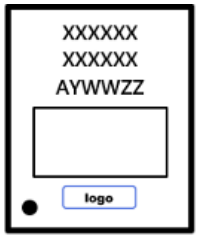


LAND PATTERN
RECOMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIT IN MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.77	0.87	0.97
A3		0.425 REF	
b	0.360	0.410	0.460
D		5.00 BSC	
D2	3.670	3.720	3.770
D3	3.600	–	4.400
D4		2.080 REF	
e		1.270 BSC	
e1		0.690 BSC	
E		6.00 BSC	
E2	3.600	3.650	3.700
E3	1.680	–	2.480
E4		0.630 REF	
E5	0.410	0.460	0.510
E6	0.415	0.465	0.515
k		1.270 REF	
L	0.415	0.465	0.515
L2		0.075 REF	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
fff		0.10	

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**PDSO-N8 5.00x6.00x0.87, 1.27P**	**PAGE 1 OF 1**

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