Small Signal MOSFET

-20 V, -280 mA, P-Channel with ESD Protection, SOT-723

Features

- Enables High Density PCB Manufacturing
- 44% Smaller Footprint than SC-89 and 38% Thinner than SC-89
- Low Voltage Drive Makes this Device Ideal for Portable Equipment
- Low Threshold Levels, 1.8 V R_{DS(on)} Rating
- Low Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels Using the Same Basic Topology.
- This is a Pb–Free Device

Applications

- Interfacing, Switching
- High Speed Switching
- Cellular Phones, PDA's

MAXIMUM RATINGS (T_J = 25° C unless otherwise stated)

Parame	ter		Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	-20	V
Gate-to-Source Voltage			V _{GS}	±8.0	V
Continuous Drain	Steady	T _A = 25°C		-260	
Current (Note 1)	State	T _A = 85°C	I _D	-185	mA
	t ≤ 5 s	T _A = 25°C		-280	
Power Dissipation	Steady			400	
(Note 1)	State	T _A = 25°C	PD		mW
	t ≤ 5 s			500	
Continuous Drain		T _A = 25°C	I _D	-215	mA
Current (Note 2)	Steady	T _A = 85°C		-155	110 (
Power Dissipation (Note 2)	State	$T_A = 25^{\circ}C$	P _D	280	mW
Pulsed Drain Current	t _p =	10 μs	I _{DM}	-310	mA
Operating Junction and Sto	T _J , T _{STG}	–55 to 150	°C		
Source Current (Body Dioc	۱ _S	-240	mA		
Lead Temperature for Sold (1/8" from case for 10 s)	ering Purp	ooses	ΤL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
- 2. Surface-mounted on FR4 board using the minimum recommended pad size.

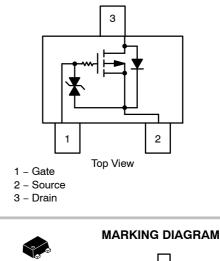


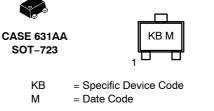
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V _{(BR)DSS}	R _{DS(on)} TYP	I _D Max
	2.7 Ω @ –4.5 V	
–20 V	4.1 Ω @ –2.5 V	–280 mA
	6.1 Ω @ –1.8 V	

SOT-723 (3-LEAD)





ORDERING INFORMATION

Device	Package	Shipping [†]
NTK3142PT1G	SOT-723 (Pb-Free)	4000/Tape & Reel 4 mm Pitch
NTK3142PT5G	SOT-723 (Pb-Free)	8000/Tape & Reel 2 mm Pitch

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Мах	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{ hetaJA}$	315	
Junction-to-Ambient $- t = 5 s$ (Note 3)	$R_{ hetaJA}$	250	°C/W
Junction-to-Ambient - Steady State Minimum Pad (Note 4)	$R_{ hetaJA}$	440	

Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
Surface-mounted on FR4 board using the minimum recommended pad size.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit		
OFF CHARACTERISTICS									
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 V, I_D = -1$	00 μΑ	-20			V		
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	$I_D = -100 \ \mu A$, Reference to $25^{\circ}C$			14		mV/°C		
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -16 V	$T_J = 25^{\circ}C$			-1.0			
		V _{DS} = -16 V	T _J = 125°C			-2.0	μΑ		
Gate-to-Source Leakage Current	I _{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V				±1	μΑ		
ON CHARACTERISTICS (Note 5)									
Gate Threshold Voltage	V _{GS(TH)}	V_{GS} = V_{DS} , I_D = -250 μ A		-0.4		-1.3	V		
Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-2.0		mV/°C		

Coefficient	VGS(TH)/ 'J		-2.0		mV/°C
Drain-to-Source On Resistance	R _{DS(ON)}	V_{GS} = -4.5V, I _D = -260 mA	2.9	4.0	Ω
Drain-to-Source On Resistance	R _{DS(ON)}	$V_{GS} = -4.5V, I_D = -10 \text{ mA}$	2.7	3.4	
		$V_{GS} = -2.5 \text{ V}, \text{ I}_{D} = -1 \text{ mA}$	4.1	5.3	Ω
		$V_{GS} = -1.8 \text{ V}, \text{ I}_{D} = -1 \text{ mA}$	6.1	10	
Forward Transconductance	9 _{FS}	$V_{DS} = -5 \text{ V}, \text{ I}_{D} = -10 \text{ mA}$	73		mS

CAPACITANCES

Input Capacitance	C _{ISS}		15.3	
Output Capacitance	C _{OSS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = -10 V	4.3	pF
Reverse Transfer Capacitance	C _{RSS}		2.3	

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 6)

Turn-On Delay Time	t _{d(ON)}		8.4	16	
Rise Time	t _r	V_{GS} = -4.5 V, V_{DD} = -5 V, I_{D} = -100 mA,	15.3	28	ns
Turn-Off Delay Time	t _{d(OFF)}	$R_{G} = 6 \Omega$	37.5	80	115
Fall Time	t _f		22.7	43	

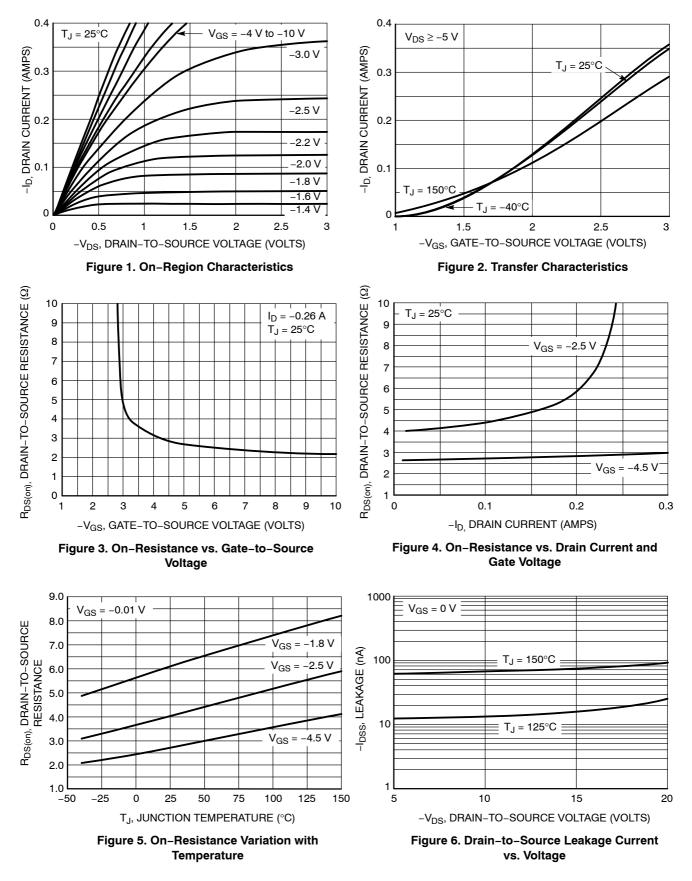
DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = –10 mA	$T_J = 25^{\circ}C$		0.69	-1.2	V	
		VGS = 0 V, IS= = 10 IIIA	T _J = 125°C		0.56			
Reverse Recovery Time	t _{RR}				37	80		
Charge Time	t _a	V _{GS} = 0 V, V _{DD} = −20 V, dI _{SD} /dt = 100 A/µs, I _S = −1.0 A			15.9	30	ns	
Discharge Time	t _b	dI _{SD} /dt = 100 A/µs, I _S		21.1	50			
Reverse Recovery Charge	Q _{RR}			20	70	nC		

5. Pulse Test: pulse width \leq 300 $\mu s,$ duty cycle \leq 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES



30 1000 $T_J = 25^{\circ}C$ $V_{GS} = 0 V$ $V_{DD} = -5 V$ $I_{\rm D} = -10 \, {\rm mA}$ 25 V_{GS} = -4.5 V C, CAPACITANCE (pF) 20 100 \dot{C}_{iss} t, TIME (ns) t_{d(off)} 15 10 t_{d(on)} 10 t, Coss 5 C_{rss} 0 1 0 2.5 5 7.5 10 12.5 15 17.5 20 1 10 100 -DRAIN-TO-SOURCE VOLTAGE (V) R_G, GATE RESISTANCE (OHMS) Figure 7. Capacitance Variation Figure 8. Resistive Switching Time Variation vs. Gate Resistance



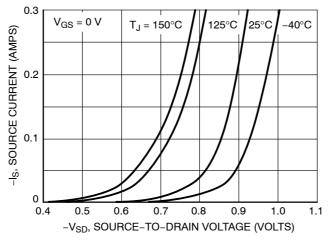


Figure 9. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



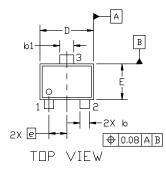
SOT-723 1.20x0.80x0.50, 0.40P CASE 631AA ISSUE E

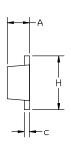
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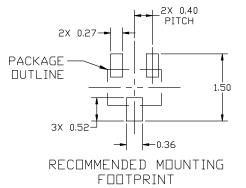
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018. CONTROLLING DIMENSION: MILLIMETERS. 1.
- 2.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH, MINIMUM З. LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



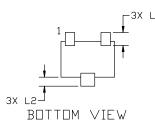


SIDE VIEW

	MILLIMETERS						
DIM	MIN.	NDM.	MAX.				
А	0.45	0.50	0.55				
b	0.15	0.21	0.27				
b1	0.25	0.31	0.37				
С	0.07	0.12	0.17				
D	1.15	1.20	1.25				
E	0.75	0.80	0.85				
e		0.40 BSC					
Н	1.15	1.20	1.25				
L	0.29 REF						
L2	0.15	0.20	0.25				



*For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.



GENERIC **MARKING DIAGRAM***



XX = Specific Device Code Μ = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 2: PIN 1. ANODE 2. N/C 3. CATHODE	STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 4: PIN 1. CATH 2. CATH 3. ANOE	ODE 2. SOURCE				
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