

Silicon Carbide (SiC) MOSFET – EliteSiC, 40 mohm, 1200 V, M1, TO-247-4L

NTH4L040N120SC1

Features

- Typ. $R_{DS(on)} = 40\text{ m}\Omega$
- Ultra Low Gate Charge ($Q_{G(tot)} = 106\text{ nC}$)
- High Speed Switching with Low Capacitance ($C_{oss} = 137\text{ pF}$)
- 100% Avalanche Tested
- $T_J = 175^\circ\text{C}$
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb-Free 2LI (on second level interconnection)

Typical Applications

- UPS
- DC-DC Converter
- Boost Inverter

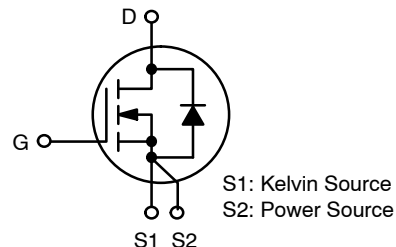
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	1200	V	
Gate-to-Source Voltage		V_{GS}	-15/+25	V	
Recommended Operation Values of Gate-to-Source Voltage		$T_C < 175^\circ\text{C}$ V_{GSop}	-5/+20	V	
Continuous Drain Current (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	I_D	58	A
			P_D	319	W
Continuous Drain Current (Notes 1, 2)	Steady State	$T_C = 100^\circ\text{C}$	I_D	41	A
			P_D	160	W
Pulsed Drain Current (Note 3)	$T_A = 25^\circ\text{C}$		I_{DM}	232	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	32	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 34\text{ A}, L = 1\text{ mH}$) (Note 4)		E_{AS}	578	mJ	
Maximum Lead Temperature for Soldering (1/8" from case for 5 s)		T_L	300	$^\circ\text{C}$	

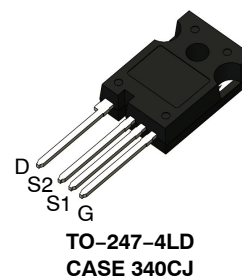
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. J_A is constant value to follow guide table of LV/HV discrete final datasheet generation.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4. EAS of 578 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 1\text{ mH}$, $I_{AS} = 34\text{ A}$, $V_{DD} = 120\text{ V}$, $V_{GS} = 20\text{ V}$.

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
1200 V	56 m Ω @ 20 V	58 A



N-CHANNEL MOSFET



MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Lot Traceability
- NTH4L040N120SC1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTH4L040N120SC1	TO-247-4LD	30 Units / Tube

NTH4L040N120SC1

Table 1. THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.47	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	1200	-	-	V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1\text{ mA}$, referenced to 25°C	-	0.45	-	V/°C	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	$T_J = 25^\circ\text{C}$	-	-	100	μA
			$T_J = 175^\circ\text{C}$	-	-	1	mA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = +25/-15\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 1	μA	

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 10\text{ mA}$	1.8	3	4.3	V
Recommended Gate Voltage	V_{GOP}		-5	-	+20	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}, I_D = 35\text{ A}, T_J = 25^\circ\text{C}$	-	40	56	m Ω
		$V_{GS} = 20\text{ V}, I_D = 35\text{ A}, T_J = 175^\circ\text{C}$	-	70	100	
Forward Transconductance	g_{FS}	$V_{DS} = 20\text{ V}, I_D = 35\text{ A}$	-	20	-	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 800\text{ V}$	-	1762	-	pF
Output Capacitance	C_{OSS}		-	137	-	
Reverse Transfer Capacitance	C_{RSS}		-	11	-	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 600\text{ V}, I_D = 47\text{ A}$	-	106	-	nC
Threshold Gate Charge	$Q_{G(TH)}$		-	16	-	
Gate-to-Source Charge	Q_{GS}		-	34	-	
Gate-to-Drain Charge	Q_{GD}		-	26	-	
Gate-Resistance	R_G	$f = 1\text{ MHz}$	-	2.4	-	Ω

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/20\text{ V}, V_{DS} = 800\text{ V}, I_D = 47\text{ A}, R_G = 4.7\text{ }\Omega$ Inductive load	-	17	30	ns
Rise Time	t_r		-	20	36	
Turn-Off Delay Time	$t_{d(OFF)}$		-	32	51	
Fall Time	t_f		-	10	20	
Turn-On Switching Loss	E_{ON}		-	411	-	μJ
Turn-Off Switching Loss	E_{OFF}		-	205	-	
Total Switching Loss	E_{tot}		-	616	-	

DRAIN-SOURCE DIODE CHARACTERISTICS

Continuous Drain-Source Diode Forward Current	I_{SD}	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$	-	-	32	A
Pulsed Drain-Source Diode Forward Current (Note 3)	I_{SDM}		-	-	232	
Forward Diode Voltage	V_{SD}	$V_{GS} = -5\text{ V}, I_{SD} = 17.5\text{ A}, T_J = 25^\circ\text{C}$	-	3.7	-	V
Reverse Recovery Time	t_{RR}	$V_{GS} = -5/20\text{ V}, I_{SD} = 47\text{ A}, dI_S/dt = 1000\text{ A}/\mu\text{s}$	-	24	-	ns
Reverse Recovery Charge	Q_{RR}		-	124.8	-	nC

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Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Energy	E_{REC}	$V_{GS} = -5/20\text{ V}$, $I_{SD} = 47\text{ A}$, $di_S/dt = 1000\text{ A}/\mu\text{s}$	-	8.4	-	μJ
Peak Reverse Recovery Current	I_{RRM}		-	10.4	-	A
Charge Time	T_a		-	12.4	-	ns
Discharge Time	T_b		-	11.6	-	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

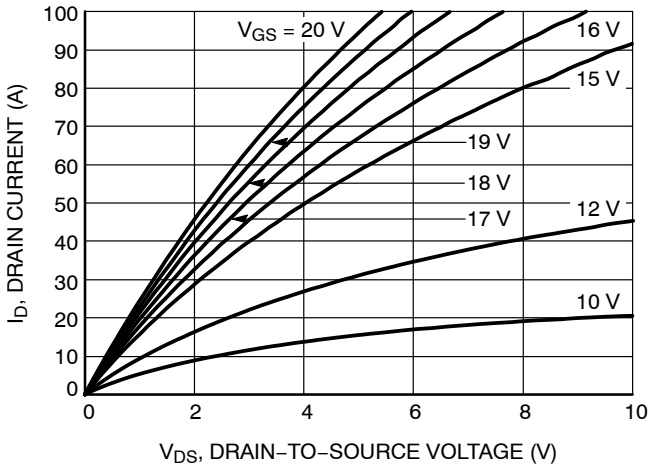


Figure 1. On-Region Characteristics

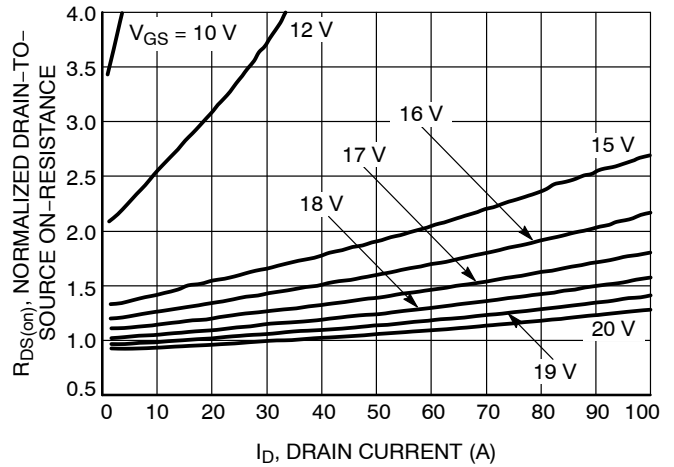


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

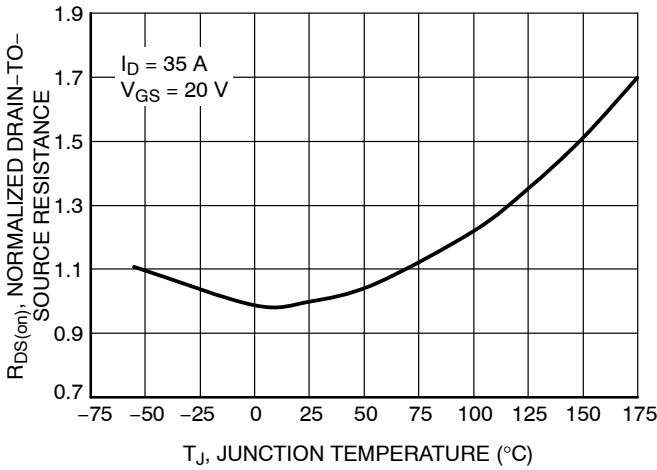


Figure 3. On-Resistance Variation with Temperature

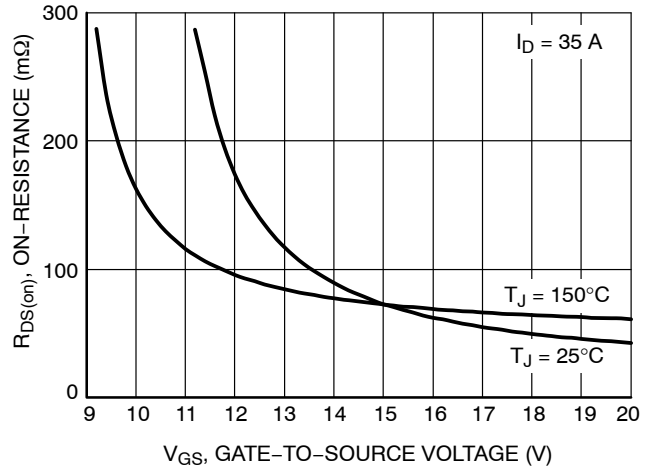


Figure 4. On-Resistance vs. Gate-to-Source Voltage

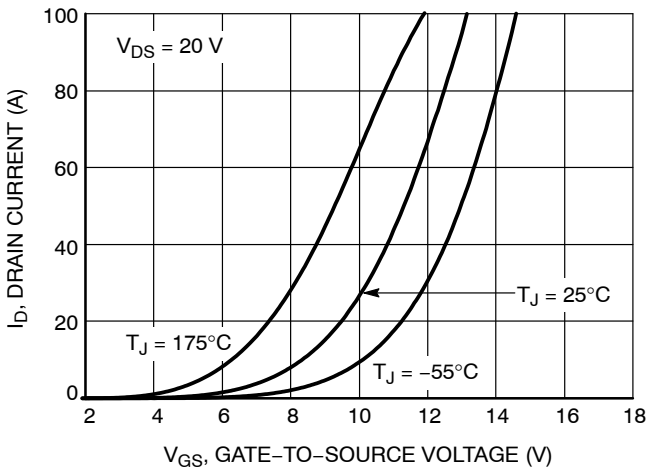


Figure 5. Transfer Characteristics

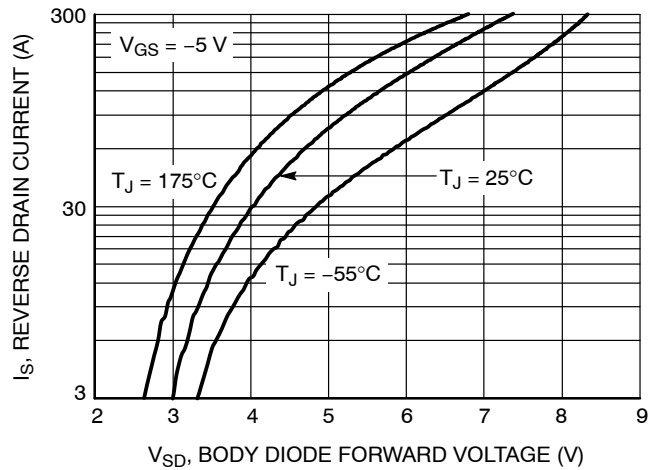


Figure 6. Diode Forward Voltage vs. Current

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TYPICAL CHARACTERISTICS (CONTINUED)

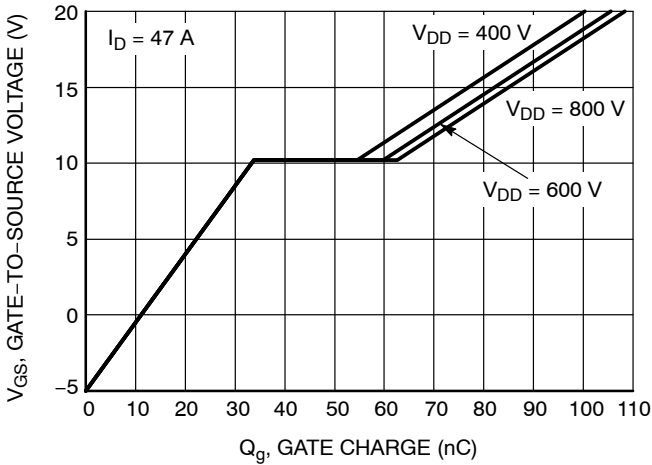


Figure 7. Gate-to-Source Voltage vs. Total Charge

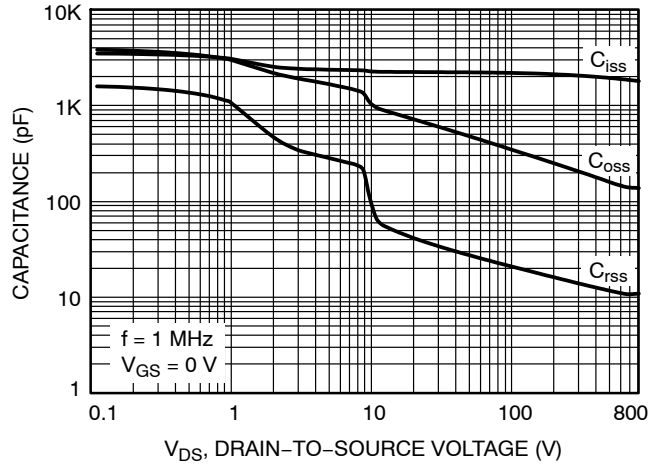


Figure 8. Capacitance vs. Drain-to-Source Voltage

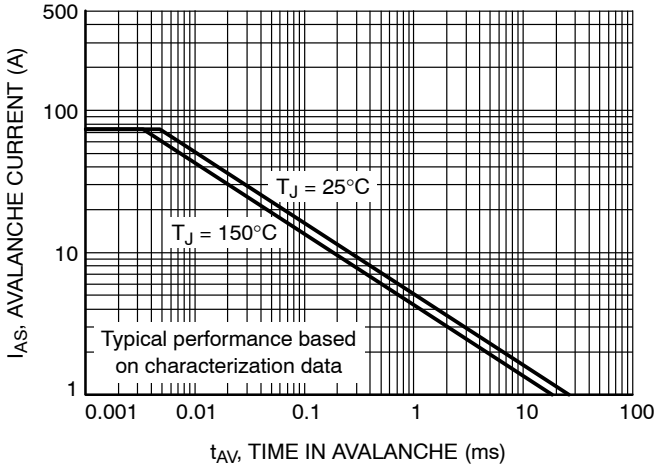


Figure 9. Unclamped Inductive Switching Capability

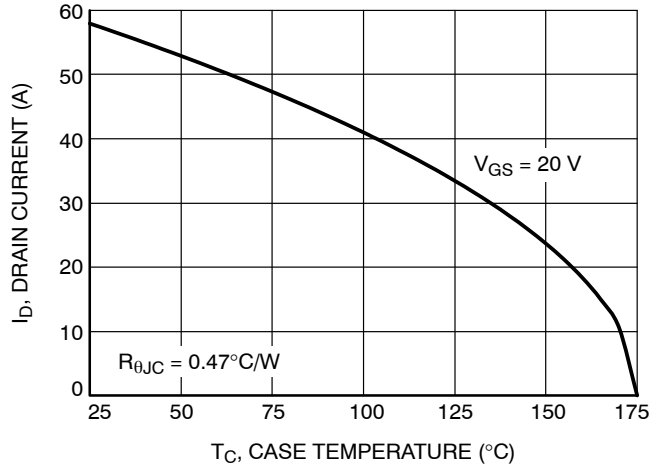


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

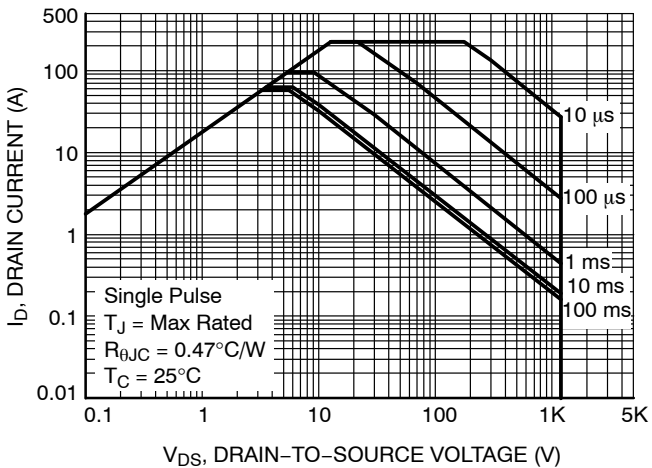


Figure 11. Safe Operating Area

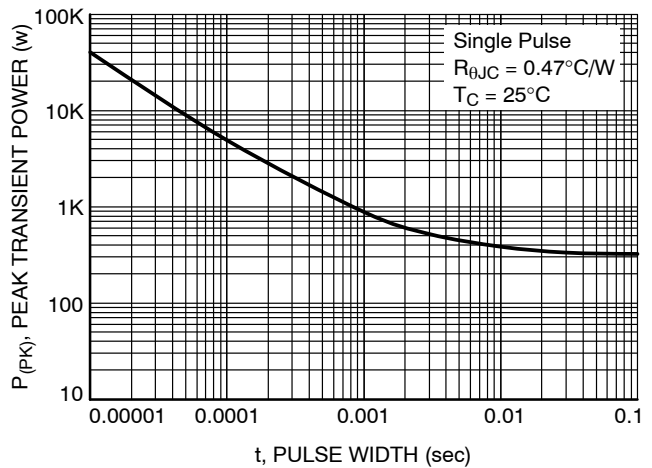


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (CONTINUED)

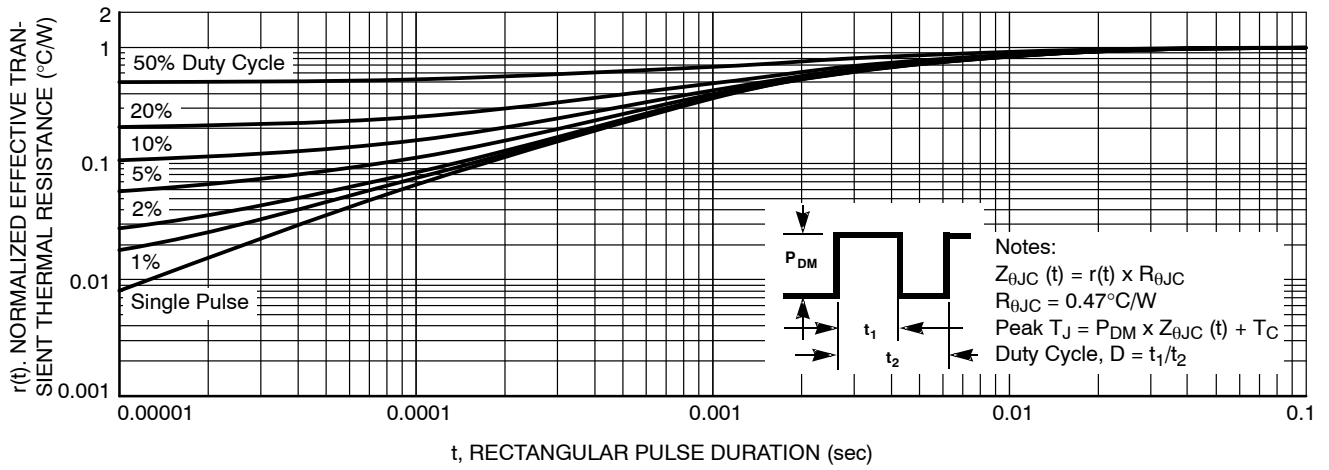


Figure 13. Junction-to-Ambient Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-4LD
CASE 340CJ
ISSUE A

DATE 16 SEP 2019



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.10	2.40	2.70
A2	1.80	2.00	2.20
b	1.07	1.20	1.33
b1	1.20	1.40	1.60
b2	2.02	2.22	2.42
c	0.50	0.60	0.70
D	22.34	22.54	22.74
D1	16.00	16.25	16.50
D2	0.97	1.17	1.37
e	2.54 BSC		
e1	5.08 BSC		
E	15.40	15.60	15.80
E1	12.80	13.00	13.20
E/2	4.80	5.00	5.20
L	18.22	18.42	18.62
L1	2.42	2.62	2.82
p	3.40	3.60	3.80
p1	6.60	6.80	7.00
Q	5.97	6.17	6.37
S	5.97	6.17	6.37

NOTES:

- A. NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5-2009.

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