

NTGS3130N, NVGS3130N

MOSFET – Single, N-Channel, TSOP-6 20 V, 5.6 A, 24 mΩ

Features

- Leading Edge Trench Technology for Low On Resistance
- Low Gate Charge for Fast Switching
- Small Size (3 x 2.75 mm) TSOP-6 Package
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

Applications

- DC-DC Converters
- Lithium Ion Battery Applications
- Load/Power Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	20	V
Gate-to-Source Voltage			V _{GS}	±8	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	5.6	A
		T _A = 85°C		4.1	
	t ≤ 10 s	T _A = 25°C		6.2	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.1	W
	t ≤ 10 s			1.4	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	4.2	A
		T _A = 85°C		3.0	
Power Dissipation (Note 2)			T _A = 25°C	P _D	0.6
Pulsed Drain Current	t _p ≤ 10 s		I _{DM}	19	A
Operating and Storage Temperature Range			T _J , T _{stg}	−55 to 150	°C
Source Current (Body Diode)			I _S	1.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	R _{θJA}	110	°C/W
Junction-to-Ambient – t ≤ 10 s (Note 1)		90	
Junction-to-Ambient – Steady State (Note 2)		200	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in sq pad size
(Cu area = 1.127 in sq [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size

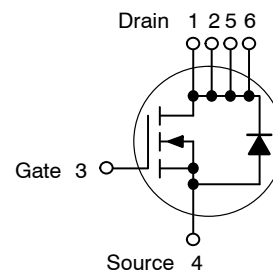


ON Semiconductor®

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V _{(BR)DSS}	R _{DS(on)} mAX	I _D Max
20 V	24 mΩ @ 4.5 V	5.6 A
	32 mΩ @ 2.5 V	4.9 A

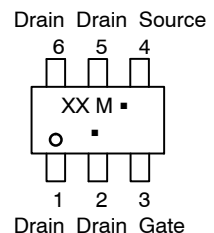
N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



TSOP-6
CASE 318G
STYLE 1



XX = Specific Device Code
M = Date Code*
■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V; I _D = 250 μA	20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			9.8		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V; V _{DS} = 16 V, T _J = 25°C			1.0	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0, V _{GS} = ±8 V			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	0.4	0.6	1.4	V
Negative Temperature Coefficient	V _{GS(TH)} /T _J			3.4		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.6 A		19	24	mΩ
		V _{GS} = 2.5 V, I _D = 4.9 A		25	32	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 5.6 A		8.2		S

CHARGES, CAPACITANCE, & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 16 V		935		pF
Output Capacitance	C _{OSS}			169		
Reverse Transfer Capacitance	C _{RSS}			104		
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 10 V		965		pF
Output Capacitance	C _{OSS}			198		
Reverse Transfer Capacitance	C _{RSS}			110		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V V _{DS} = 16 V I _D = 5.6 A		13.2	20.3	nC
Threshold Gate Charge	Q _{G(TH)}			0.60		
Gate-to-Source Charge	Q _{GS}			1.5		
Gate-to-Drain Charge	Q _{GD}			4.2		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V V _{DS} = 5.0 V I _D = 6.2 A		11.8	18.0	
Threshold Gate Charge	Q _{G(TH)}			0.6		
Gate-to-Source Charge	Q _{GS}			1.4		
Gate-to-Drain Charge	Q _{GD}			2.7		

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DD} = 16 V, I _D = 1 A, R _G = 3 Ω		6.3	12.6	ns
Rise Time	t _r			7.3	13.5	
Turn-Off Delay Time	t _{d(OFF)}			21.7	35.1	
Fall Time	t _f			9.7	17.6	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1.0 A	T _J = 25°C		0.7	1.2	V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 Vdc, dI _{SD} /dt = 100 A/μs, I _S = 1.0 A			20.4		ns
Charge Time	t _a				8.1		
Discharge Time	t _b				11.6		
Reverse Recovery Charge	Q _{RR}				8.8		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperature.

NTGS3130N, NVGS3130N

TYPICAL CHARACTERISTICS

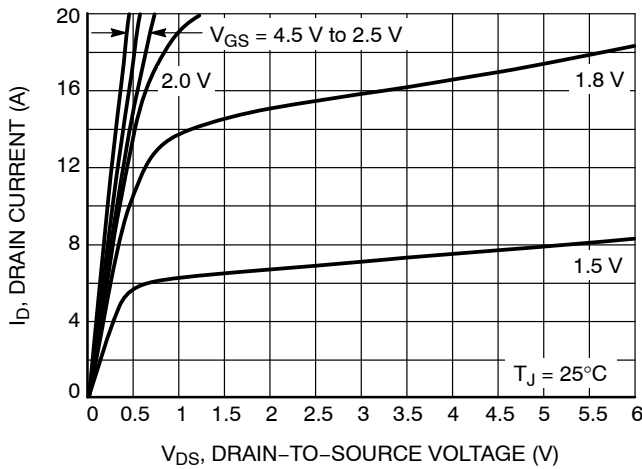


Figure 1. On-Region Characteristics

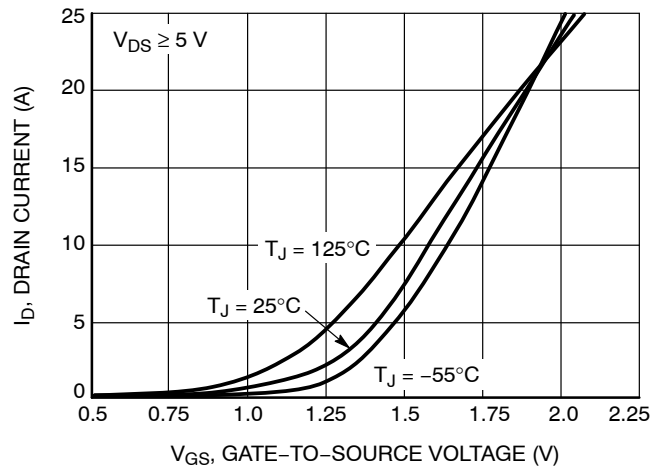


Figure 2. Transfer Characteristics

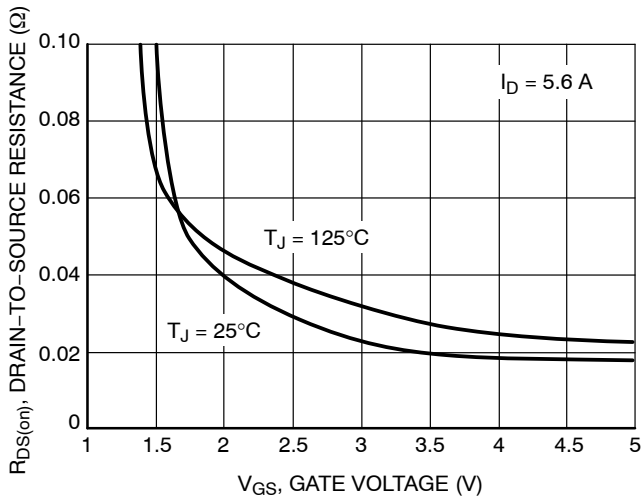


Figure 3. On-Resistance vs. Gate-to-Source Voltage

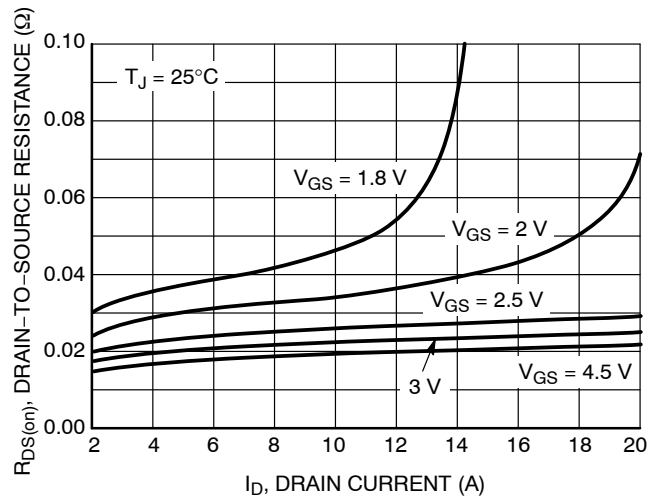


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

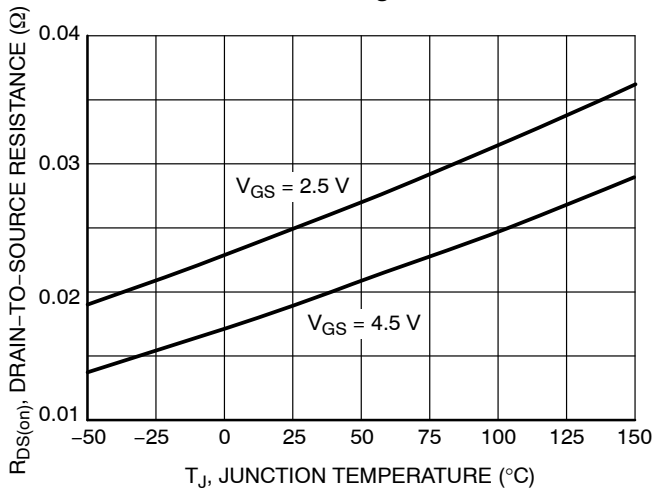


Figure 5. On-Resistance Variation with Temperature

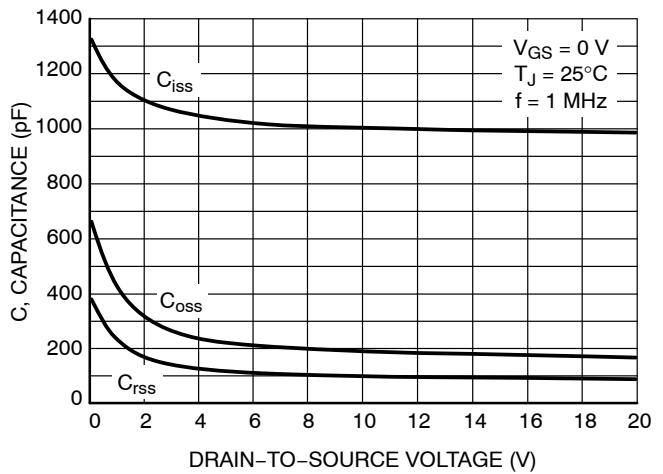


Figure 6. Capacitance Variation

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TYPICAL CHARACTERISTICS

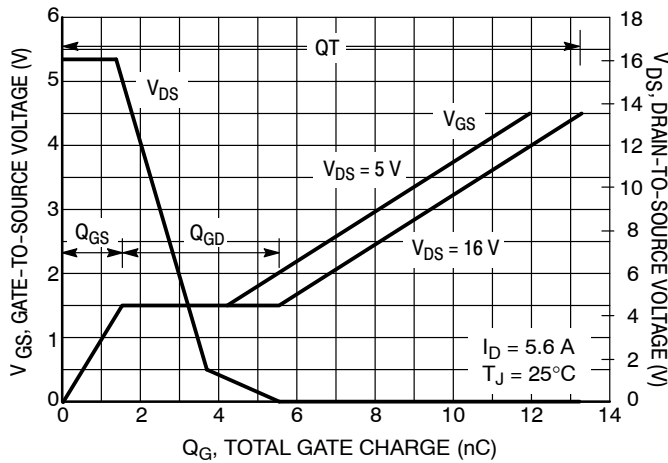


Figure 7. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

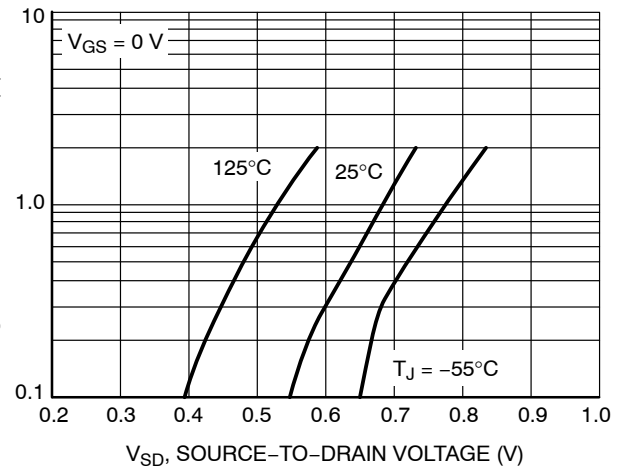


Figure 8. Diode Forward Voltage vs. Current

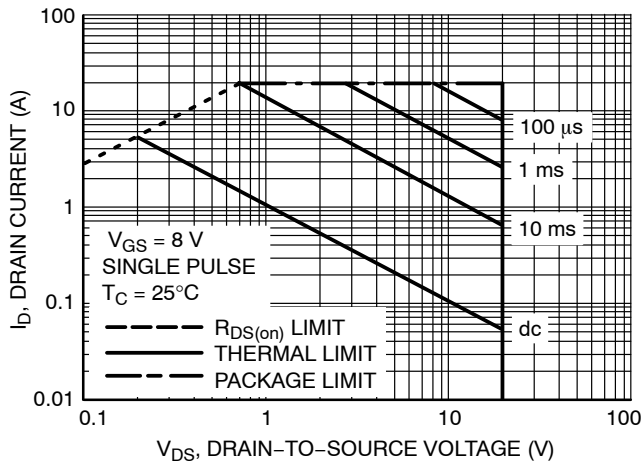


Figure 9. Maximum Rated Forward Biased Safe Operating Area

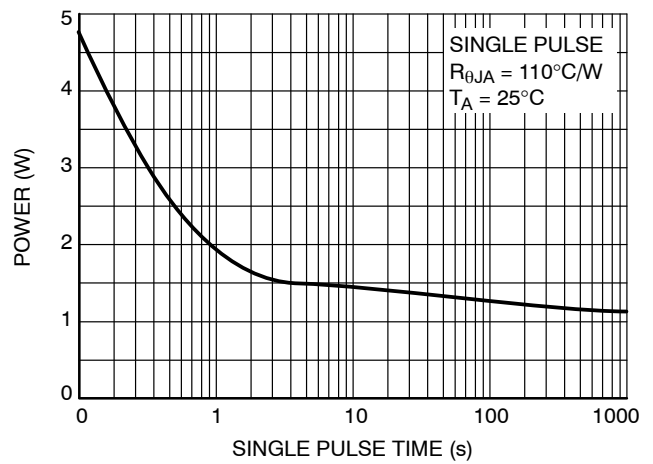


Figure 10. Single Pulse Maximum Power Dissipation

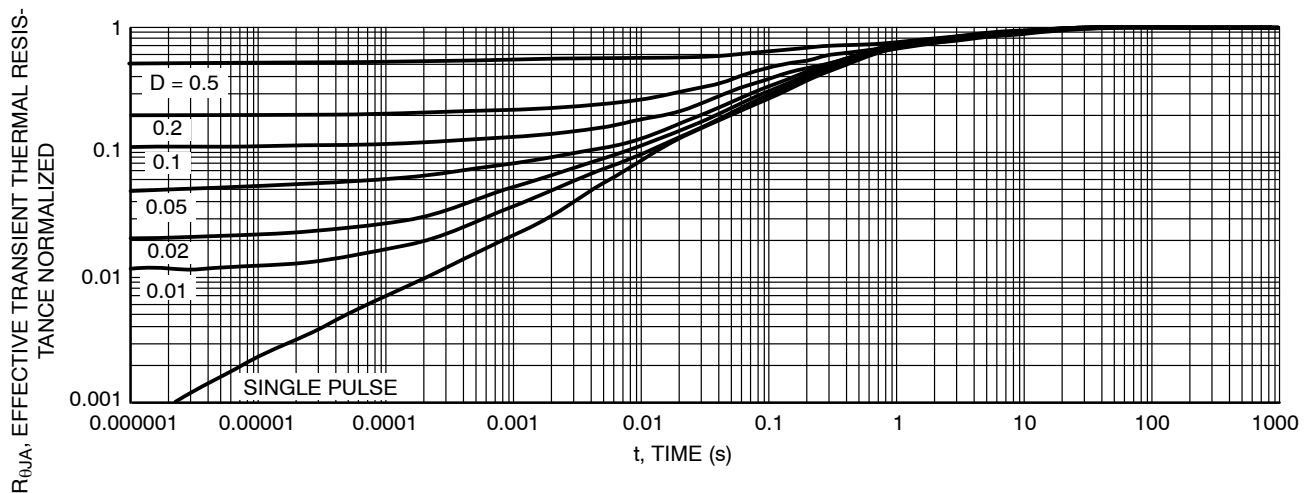


Figure 11. Thermal Response

NTGS3130N, NVGS3130N

Table 1. ORDERING INFORMATION

Part Number	Marking (XX)	Package	Shipping[†]
NTGS3130NT1G	S9	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NVGS3130NT1G	VS9	TSOP-6 (Pb-Free)	3000 / Tape & Reel

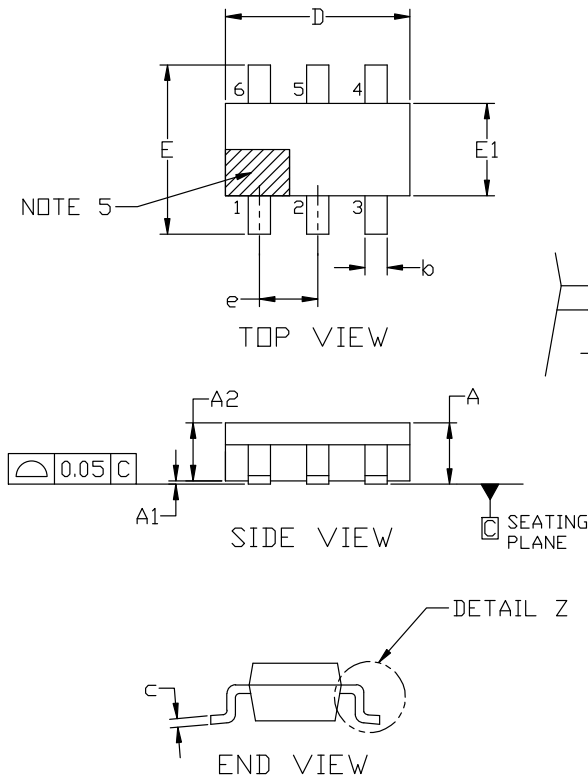
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



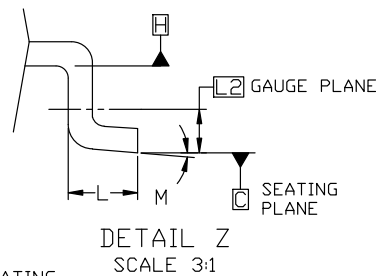
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

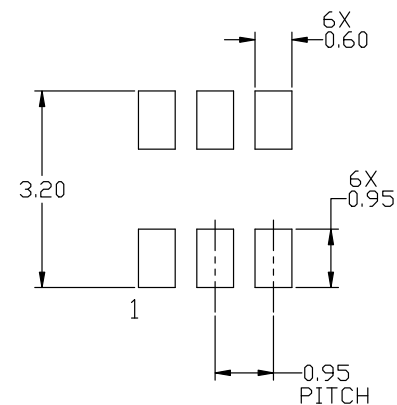


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



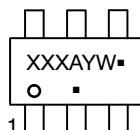
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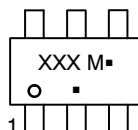
ISSUE W

DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

▪ = Pb-Free Package

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:

PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:

PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:

PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:

PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:

PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:

PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:

PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:

PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:

PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+

STYLE 11:

PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:

PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:

PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:

PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:

PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:

PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:

PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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