

# NTGD4167C

## MOSFET – POWER, Dual, Complementary, TSOP-6 30 V, +2.9/-2.2 A

### Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size (3 x 3 mm) Dual TSOP-6 Package
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb-Free Device

### Applications

- DC-DC Conversion Circuits
- Load/Power Switching with Level Shift

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	30	V
Gate-to-Source Voltage (N-Ch & P-Ch)			V <sub>GS</sub>	±12	V
N-Channel Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C T <sub>A</sub> = 85°C	I <sub>D</sub>	2.6 1.9	A
	t ≤ 5 s	T <sub>A</sub> = 25°C		2.9	
	P-Channel Continuous Drain Current (Note 1)	Steady State		T <sub>A</sub> = 25°C T <sub>A</sub> = 85°C	
t ≤ 5 s		T <sub>A</sub> = 25°C	-2.2		
Power Dissipation (Note 1)		Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.9
	t ≤ 5 s	1.1			
Pulsed Drain Current	N-Ch	t <sub>p</sub> = 10 μs	I <sub>DM</sub>	8.6	A
	P-Ch			-6.3	
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
Source Current (Body Diode)			I <sub>S</sub>	±0.9	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	R <sub>θJA</sub>	140	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 1)	R <sub>θJA</sub>	110	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

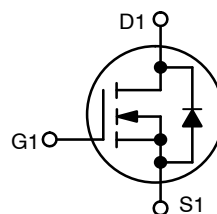
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



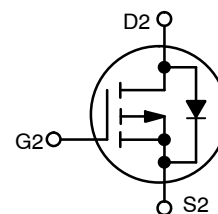
ON Semiconductor®

<http://onsemi.com>

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX (Note 1)
N-Ch 30 V	90 mΩ @ 4.5 V	2.6 A
	125 mΩ @ 2.5 V	2.2 A
P-Ch -30 V	170 mΩ @ -4.5 V	-1.9 A
	300 mΩ @ -2.5 V	-1.0 A



N-CHANNEL MOSFET

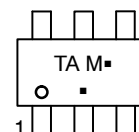


P-CHANNEL MOSFET



TSOP-6  
CASE 318G  
STYLE 13

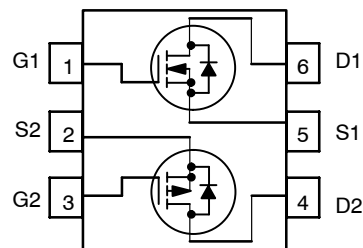
### MARKING DIAGRAM



TA = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTION



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

# NTGD4167C

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	N	V <sub>GS</sub> = 0 V	I <sub>D</sub> = 250 μA	30			V
		P		I <sub>D</sub> = -250 μA	-30			
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	N				21.4		mV/°C
		P				22.2		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	N	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25 °C			1.0	μA
		P	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -24 V				-1.0	
		N	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 85 °C			10	
		P	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -24 V				-10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	N	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V				±100	nA
		P	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V				±100	

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	N	V <sub>GS</sub> = V <sub>DS</sub>	I <sub>D</sub> = 250 μA	0.5	0.9	1.5	V
		P		I <sub>D</sub> = -250 μA	-0.5	-1.1	-1.5	
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	N	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.6 A			52	90	mΩ
			V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 2.2 A			67	125	
		P	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.9 A			130	170	
			V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1.0 A			202	300	
Forward Transconductance	g <sub>FS</sub>	N	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.6 A			2.6		S
		P	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1.9 A			2.6		

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	N	f = 1 MHz, V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 15 V		295		pF
Output Capacitance	C <sub>OSS</sub>					48		
Reverse Transfer Capacitance	C <sub>RSS</sub>					27		
Input Capacitance	C <sub>ISS</sub>	P		V <sub>DS</sub> = -15 V		419		
Output Capacitance	C <sub>OSS</sub>					51		
Reverse Transfer Capacitance	C <sub>RSS</sub>					26		
Total Gate Charge	Q <sub>G(TOT)</sub>	N	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.0 A			3.7	5.5	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>					0.6		
Gate-to-Source Gate Charge	Q <sub>GS</sub>					0.9		
Gate-to-Drain “Miller” Charge	Q <sub>GD</sub>					0.8		
Total Gate Charge	Q <sub>G(TOT)</sub>	P	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.0 A			3.9	6.0	
Threshold Gate Charge	Q <sub>G(TH)</sub>					0.6		
Gate-to-Source Gate Charge	Q <sub>GS</sub>					1.0		
Gate-to-Drain “Miller” Charge	Q <sub>GD</sub>					1.0		

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	N	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1.0 A, R <sub>G</sub> = 6.0 Ω		7.0		ns
Rise Time	t <sub>r</sub>				4.0		
Turn-Off Delay Time	t <sub>d(OFF)</sub>				14		
Fall Time	t <sub>f</sub>				2.0		
Turn-On Delay Time	t <sub>d(ON)</sub>	P	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -1.0 A, R <sub>G</sub> = 6.0 Ω		8.0		
Rise Time	t <sub>r</sub>				8.0		
Turn-Off Delay Time	t <sub>d(OFF)</sub>				22		
Fall Time	t <sub>f</sub>				8.0		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

# NTGD4167C

3. Switching characteristics are independent of operating junction temperatures.

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit	
DRAIN-SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V <sub>SD</sub>	N	V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25 °C	I <sub>S</sub> = 0.9 A		0.7	1.2	V
		P		I <sub>S</sub> = -0.9 A		-0.8	-1.2	
Reverse Recovery Time	t <sub>RR</sub>	N	V <sub>GS</sub> = 0 V, dI <sub>S</sub> / dt = 100 A/μs, I <sub>S</sub> = 0.9 A		8.0		ns	
Charge Time	t <sub>a</sub>				5.0			
Discharge Time	t <sub>b</sub>				3.0			
Reverse Recovery Charge	Q <sub>RR</sub>				3.0		nC	
Reverse Recovery Time	t <sub>RR</sub>	P	V <sub>GS</sub> = 0 V, dI <sub>S</sub> / dt = 100 A/μs, I <sub>S</sub> = -0.9 A		12		ns	
Charge Time	t <sub>a</sub>				10			
Discharge Time	t <sub>b</sub>				2.0			
Reverse Recovery Charge	Q <sub>RR</sub>				7.0		nC	

N-CHANNEL TYPICAL CHARACTERISTICS

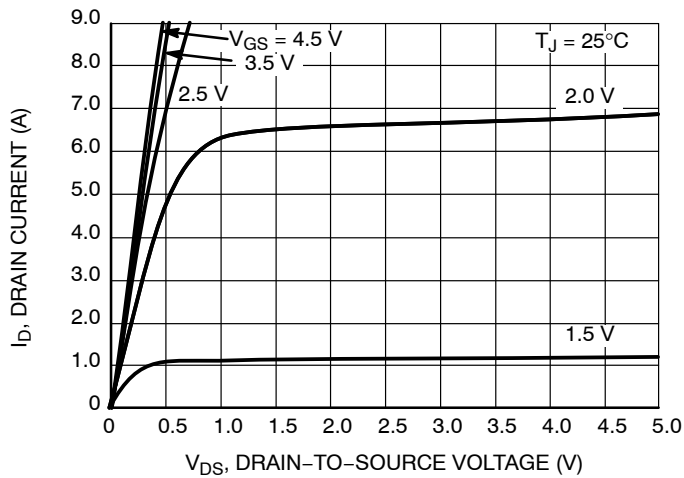


Figure 1. On-Region Characteristics

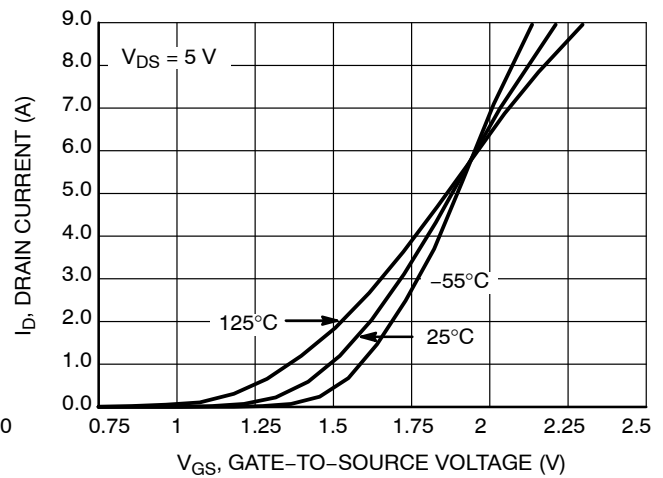


Figure 2. Transfer Characteristics

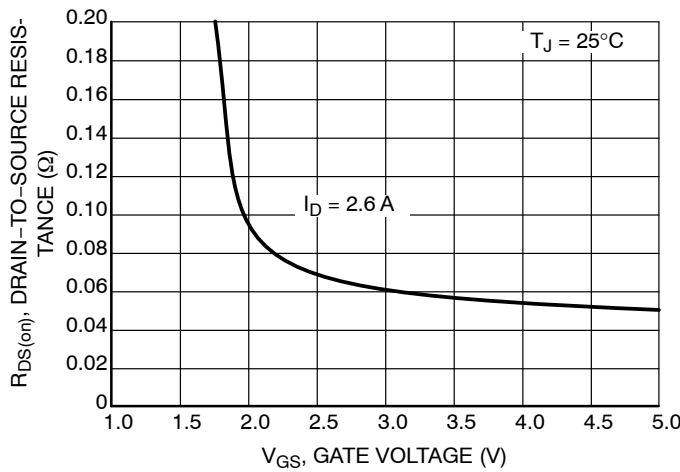


Figure 3. On-Region vs. Gate-To-Source Voltage

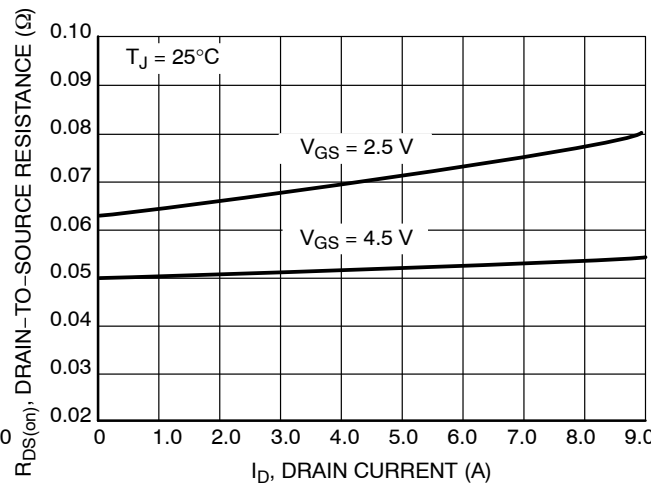


Figure 4. On-Resistance vs. Drain Current and Temperature

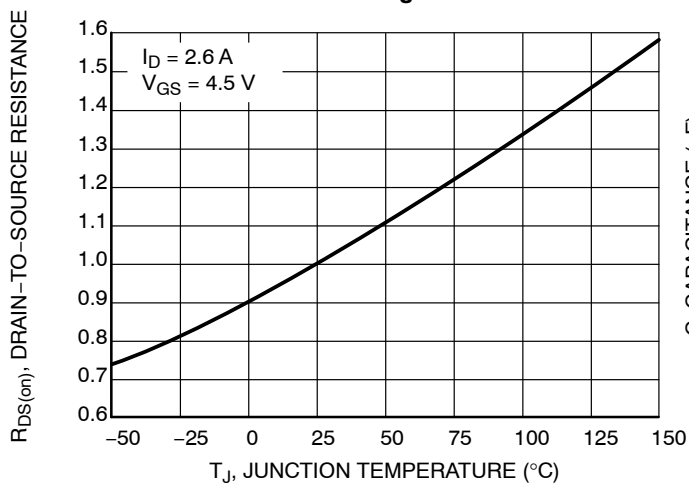


Figure 5. On-Resistance Variation with Temperature

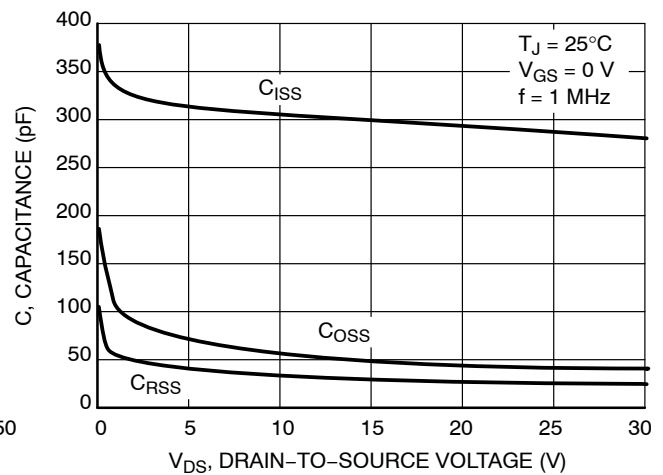
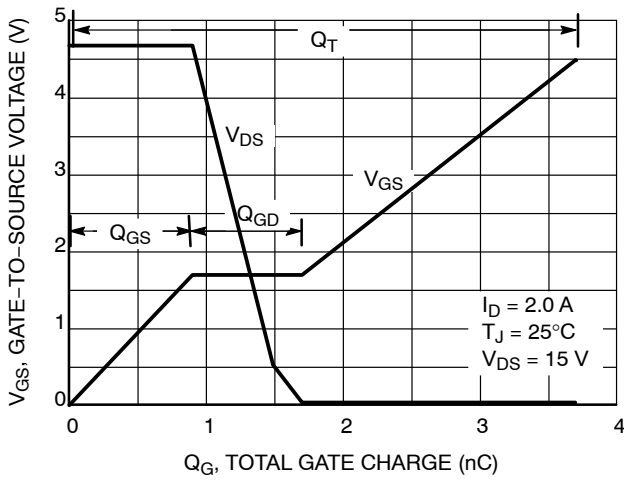
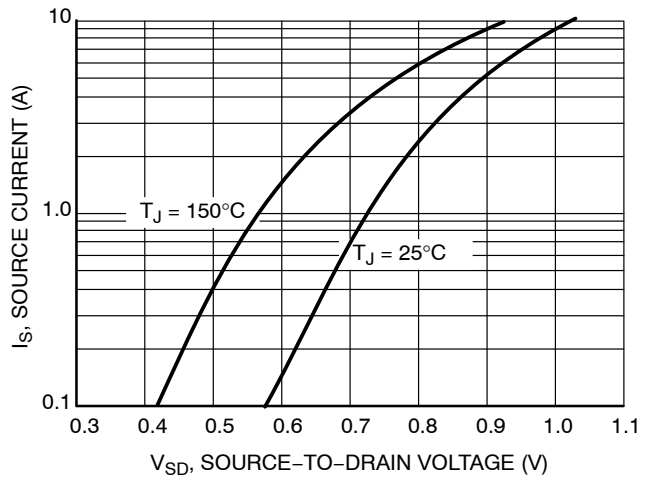


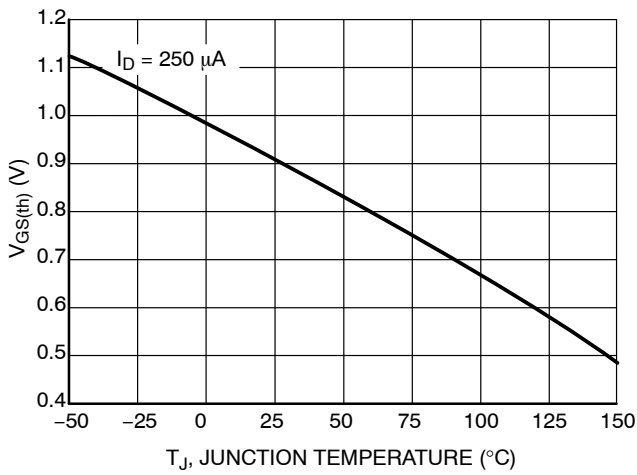
Figure 6. Capacitance Variation



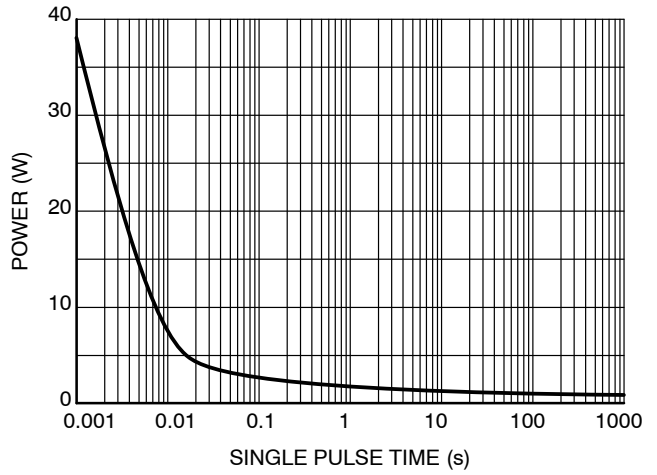
**Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



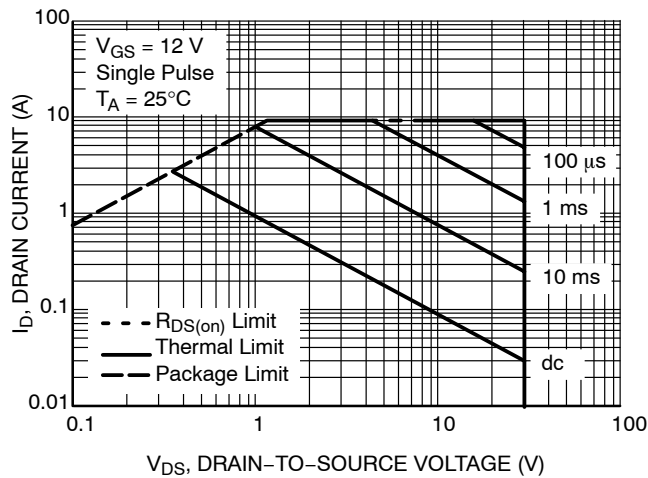
**Figure 8. Diode Forward Voltage versus Current**



**Figure 9. Threshold Voltage**



**Figure 10. Single Pulse Maximum Power Dissipation**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

# NTGD4167C

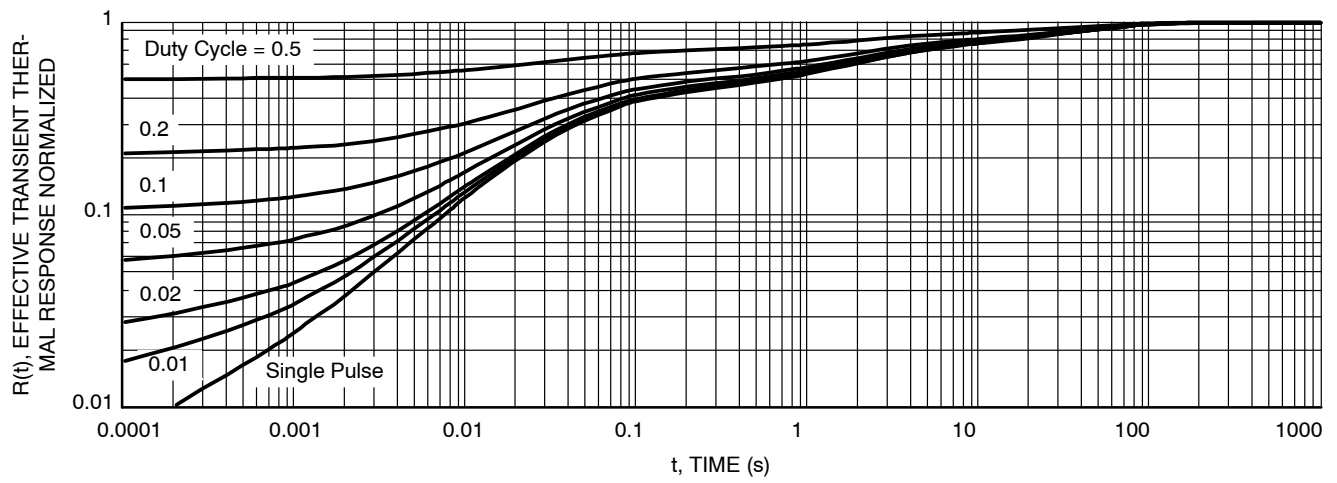


Figure 12. FET Thermal Response

P-CHANNEL TYPICAL CHARACTERISTICS

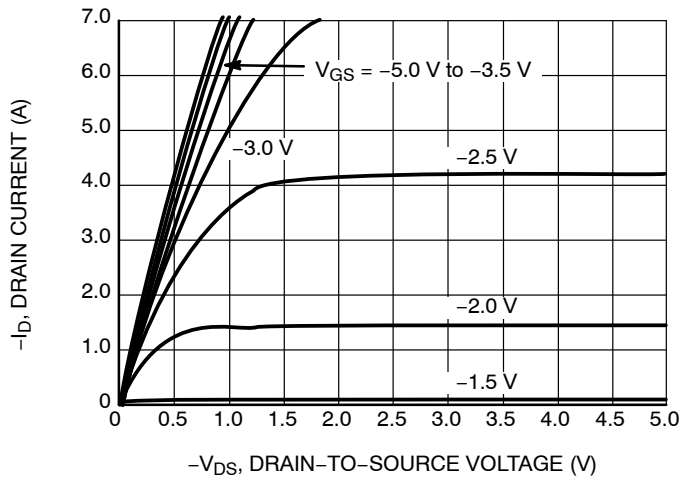


Figure 13. On-Region Characteristics

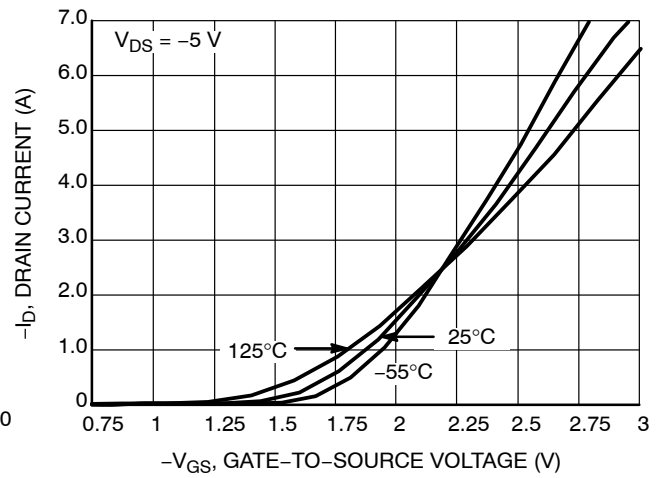


Figure 14. Transfer Characteristics

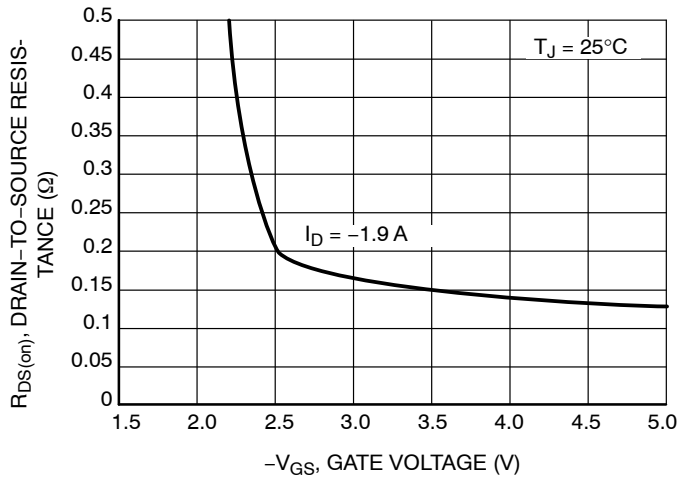


Figure 15. On-Region vs. Gate-To-Source Voltage

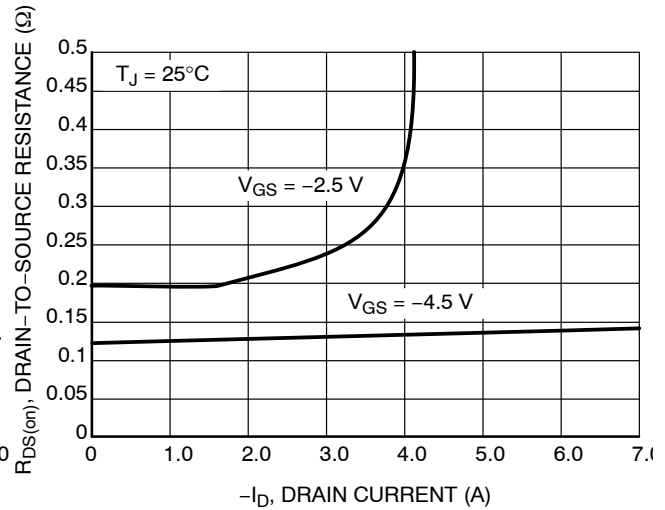


Figure 16. On-Resistance vs. Drain Current and Temperature

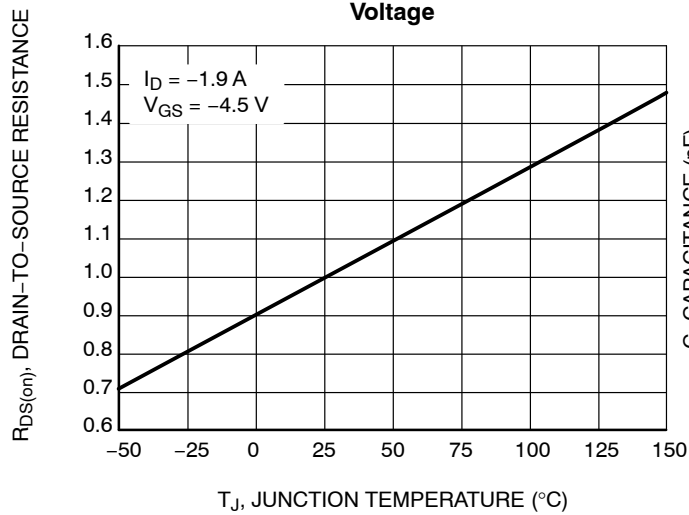


Figure 17. On-Resistance Variation with Temperature

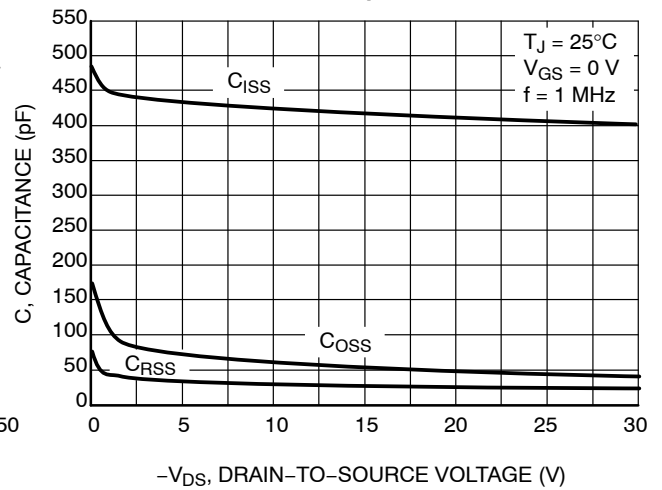
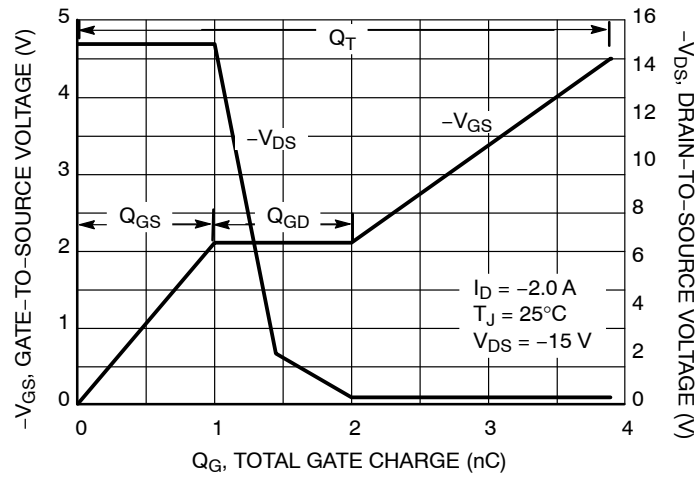
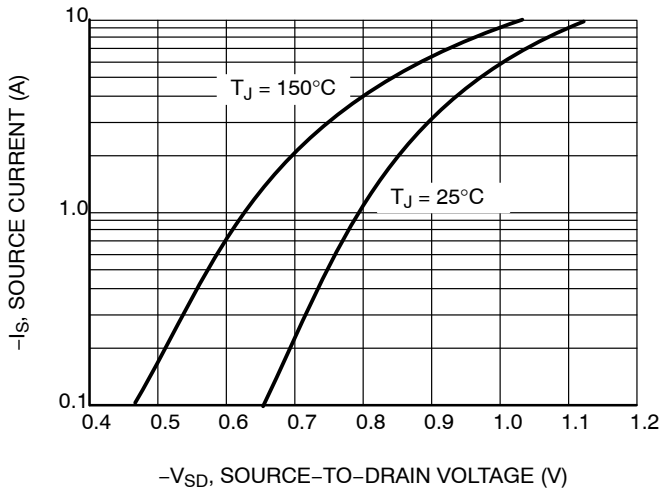


Figure 18. Capacitance Variation

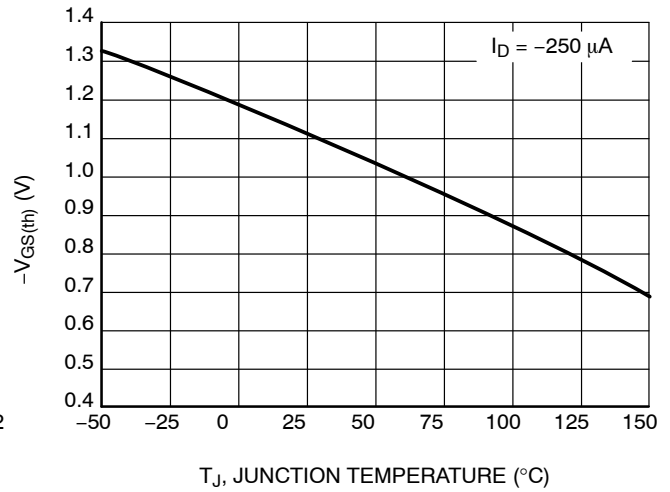
# NTGD4167C



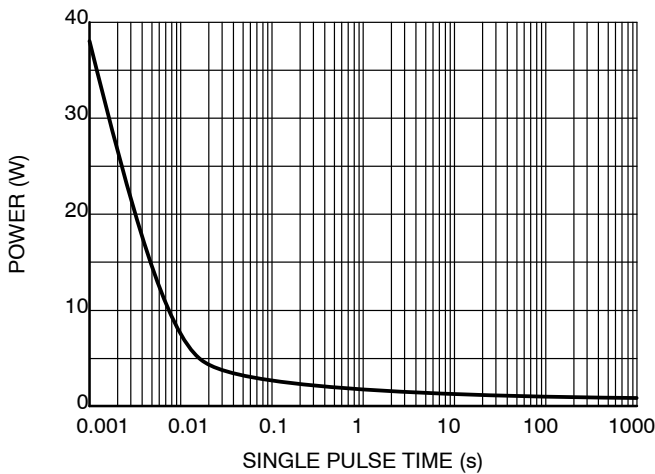
**Figure 19. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



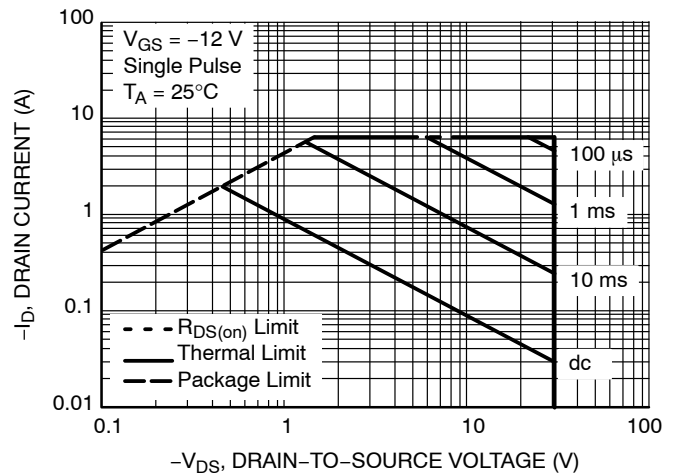
**Figure 20. Diode Forward Voltage versus Current**



**Figure 21. Threshold Voltage**



**Figure 22. Single Pulse Maximum Power Dissipation**



**Figure 23. Maximum Rated Forward Biased Safe Operating Area**



# NTGD4167C

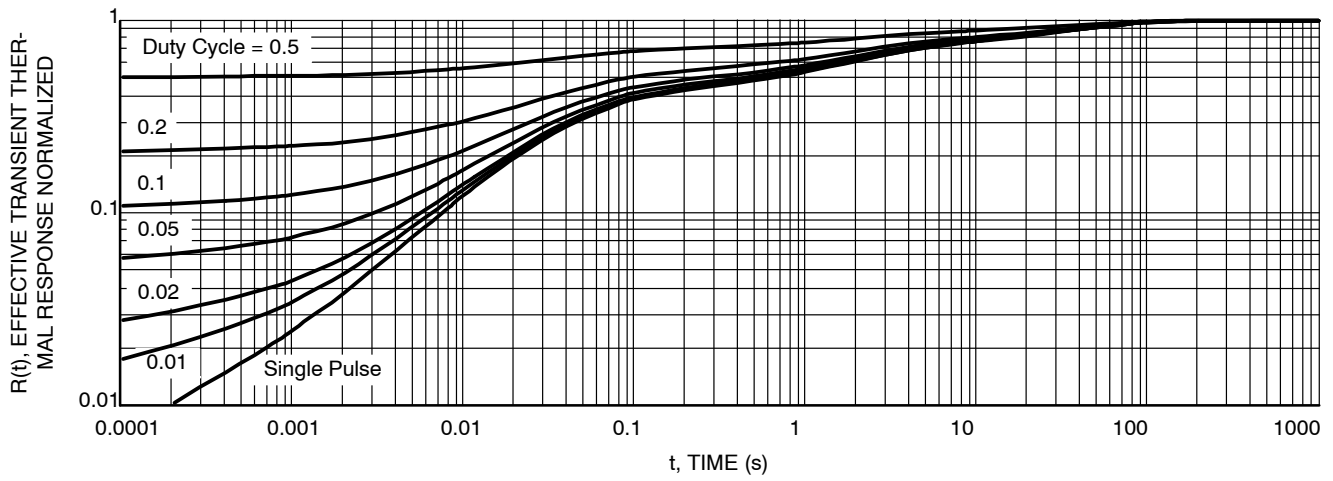


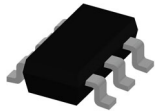
Figure 24. FET Thermal Response

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTGD4167CT1G	TSOP6 (Pb-Free)	3000 / Tape & Reel

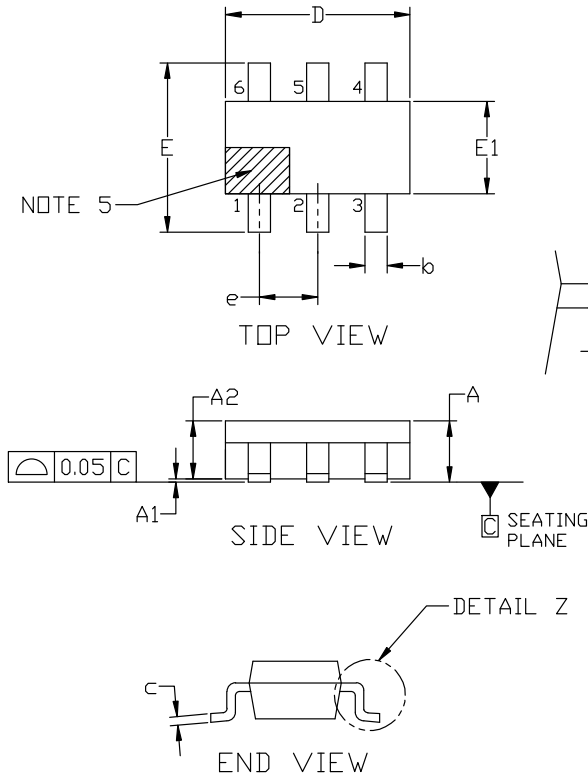
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



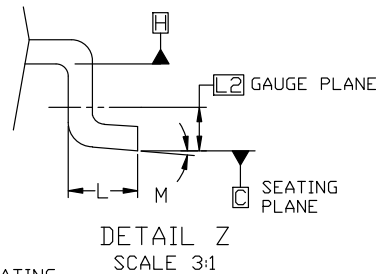
**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

**DATE 26 FEB 2024**

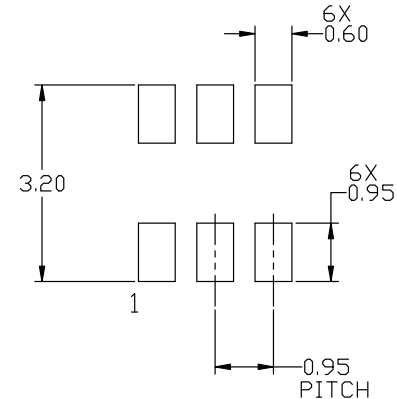


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



## RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98ASB14888C</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TSOP-6 3.00x1.50x0.90, 0.95P</b>	<b>PAGE 1 OF 2</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



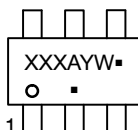
TSOP-6 3.00x1.50x0.90, 0.95P

CASE 318G

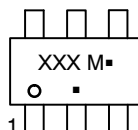
ISSUE W

DATE 26 FEB 2024

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

▪ = Pb-Free Package

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

#### STYLE 1:

PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

#### STYLE 2:

PIN 1. EMITTER 2  
2. BASE 1  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 2  
6. COLLECTOR 2

#### STYLE 3:

PIN 1. ENABLE  
2. N/C  
3. R BOOST  
4. Vz  
5. V in  
6. V out

#### STYLE 4:

PIN 1. N/C  
2. V in  
3. NOT USED  
4. GROUND  
5. ENABLE  
6. LOAD

#### STYLE 5:

PIN 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2

#### STYLE 6:

PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

#### STYLE 7:

PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. N/C  
5. COLLECTOR  
6. EMITTER

#### STYLE 8:

PIN 1. Vbus  
2. D(in)  
3. D(in)+  
4. D(out)+  
5. D(out)  
6. GND

#### STYLE 9:

PIN 1. LOW VOLTAGE GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN  
5. DRAIN  
6. HIGH VOLTAGE GATE

#### STYLE 10:

PIN 1. D(OUT)+  
2. GND  
3. D(OUT)-  
4. D(IN)-  
5. VBUS  
6. D(IN)+

#### STYLE 11:

PIN 1. SOURCE 1  
2. DRAIN 2  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 1  
6. DRAIN 1/GATE 2

#### STYLE 12:

PIN 1. I/O  
2. GROUND  
3. I/O  
4. I/O  
5. VCC  
6. I/O

#### STYLE 13:

PIN 1. GATE 1  
2. SOURCE 2  
3. GATE 2  
4. DRAIN 2  
5. SOURCE 1  
6. DRAIN 1

#### STYLE 14:

PIN 1. ANODE  
2. SOURCE  
3. GATE  
4. CATHODE/DRAIN  
5. CATHODE/DRAIN  
6. CATHODE/DRAIN

#### STYLE 15:

PIN 1. ANODE  
2. SOURCE  
3. GATE  
4. DRAIN  
5. N/C  
6. CATHODE

#### STYLE 16:

PIN 1. ANODE/CATHODE  
2. BASE  
3. EMITTER  
4. COLLECTOR  
5. ANODE  
6. CATHODE

#### STYLE 17:

PIN 1. EMITTER  
2. BASE  
3. ANODE/CATHODE  
4. ANODE  
5. CATHODE  
6. COLLECTOR

DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP-6 3.00x1.50x0.90, 0.95P	PAGE 2 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)