NTF3055L175

Power MOSFET
2.0 A, 60 V, Logic Level

N−Channel SOT−223

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- This is a Pb−Free Device

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	60	Vdc
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate−to−Source Voltage Continuous Non−repetitive ($t_p \le 10$ ms)	V_{GS}	 ± 15 ± 20	 Vdc Vpk
Drain Current Continuous @ T_A = 25°C Continuous @ T_A = 100°C Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 2.0 1.2 6.0	 Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2) Derate above 25°C	P_D	2.1 1.3 0.014	W W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, $I_{L(pk)}$ = 3.6 A, L = 10 mH, V_{DS} = 60 Vdc)	E_{AS}	65	mJ
Thermal Resistance Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JA}$ $R_{\theta JA}$	 72.3 114	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1″ pad size, 1 oz. (Cu. Area 0.995 in^2).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2−2.4 oz. (Cu. Area 0.272 in^2).

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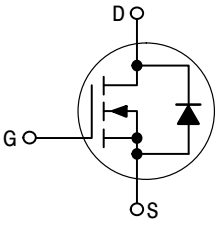
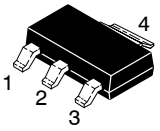
2.0 AMPERES, 60 VOLTS
$R_{DS(on)}$ = 175 mΩ

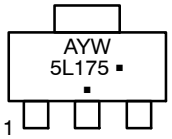
N−Channel





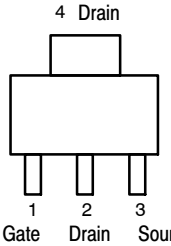
SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
5L175 = Device Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 –	 72.8 74.4	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	± 100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 –	 1.7 4.2	 2.0 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	–	155	175	mΩ
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 2.0 Adc) (V_{GS} = 5.0 Vdc, I_D = 1.0 Adc, T_J = 150°C)		$V_{DS(on)}$	–	 0.32 0.57	 0.42 –	Vdc
Forward Transconductance (Note 3) (V_{DS} = 8.0 Vdc, I_D = 1.5 Adc)		g_{fs}	–	3.2	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	–	194	270	pF
Output Capacitance		C_{oss}	–	70	100	
Transfer Capacitance		C_{rss}	–	29	40	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 2.0 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 3)	$t_{d(on)}$	–	10.2	20	ns
Rise Time		t_r	–	21	40	
Turn−Off Delay Time		$t_{d(off)}$	–	14.3	30	
Fall Time		t_f	–	15.3	30	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 2.0 Adc, V_{GS} = 5.0 Vdc) (Note 3)	Q_T	–	5.1	10	nC
		Q_1	–	1.4	–	
		Q_2	–	2.5	–	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 3)	V_{SD}	 – –	 0.84 0.68	 1.0 –	Vdc
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	–	28.3	–	ns
		t_a	–	15.6	–	
		t_b	–	12.7	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.027	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

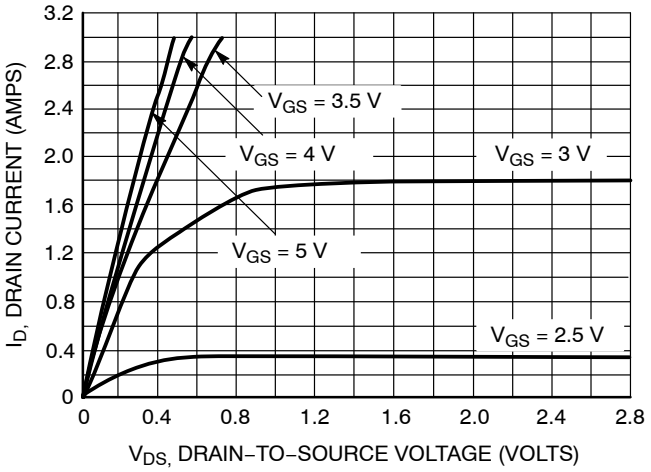


Figure 1. On−Region Characteristics

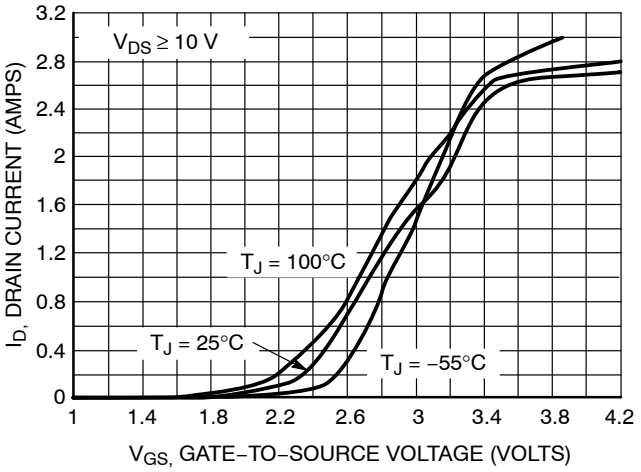


Figure 2. Transfer Characteristics

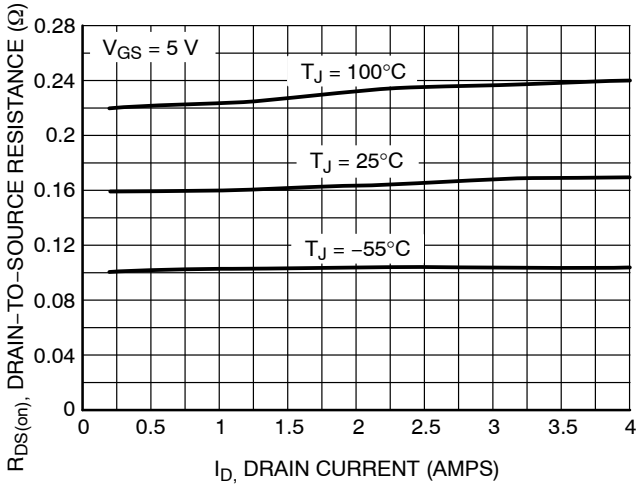


Figure 3. On−Resistance versus Gate−to−Source Voltage

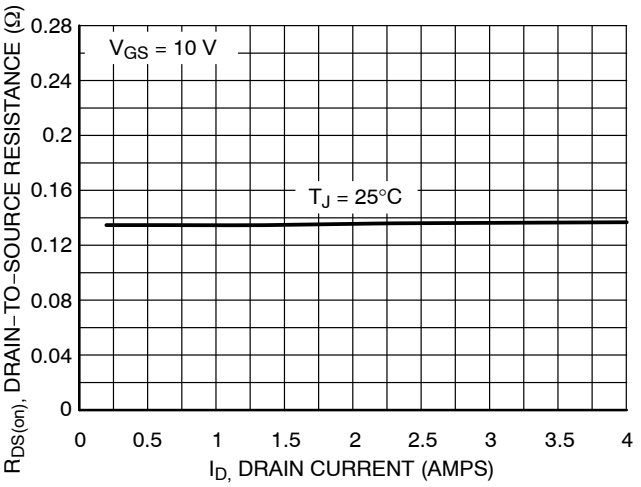


Figure 4. On−Resistance versus Drain Current and Gate Voltage

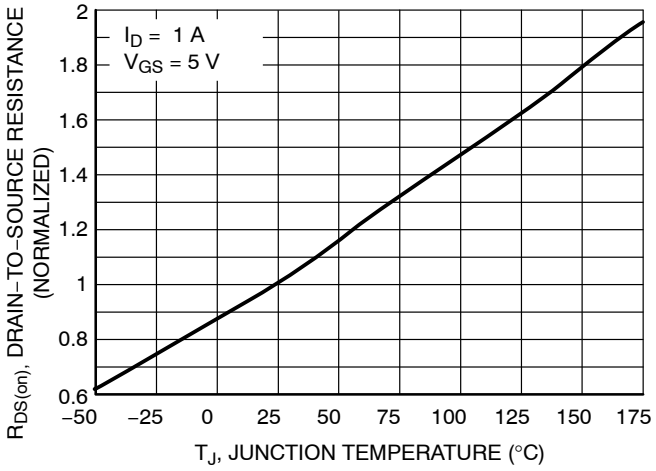


Figure 5. On−Resistance Variation with Temperature

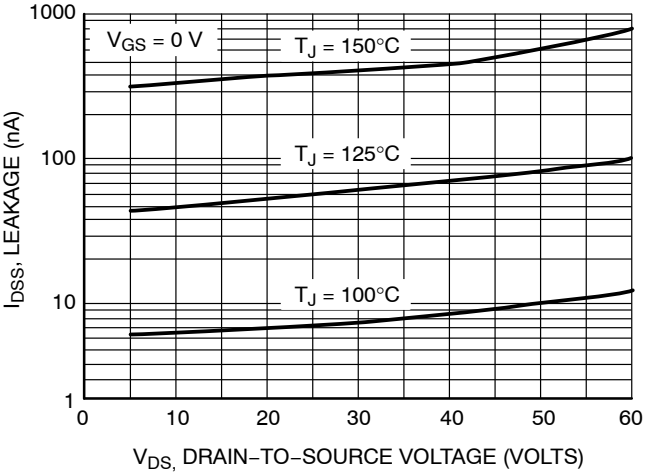


Figure 6. Drain−to−Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

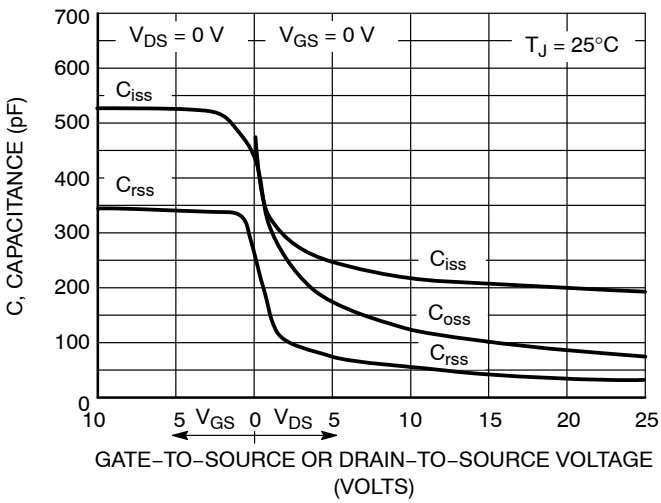


Figure 7. Capacitance Variation

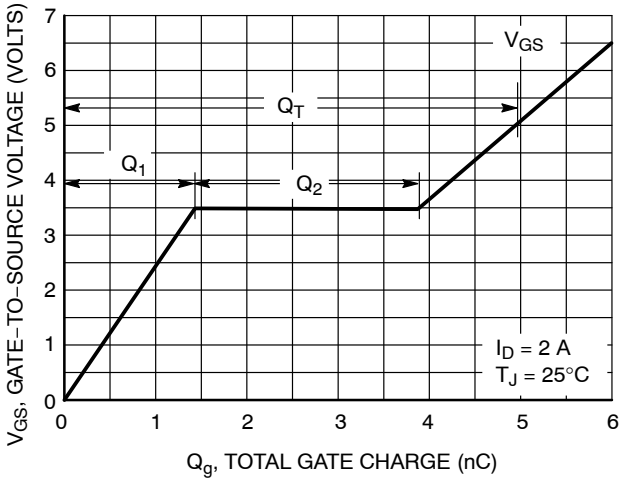


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

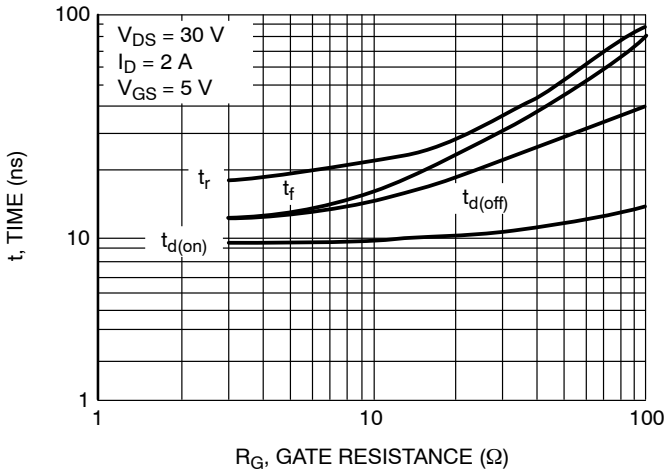


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

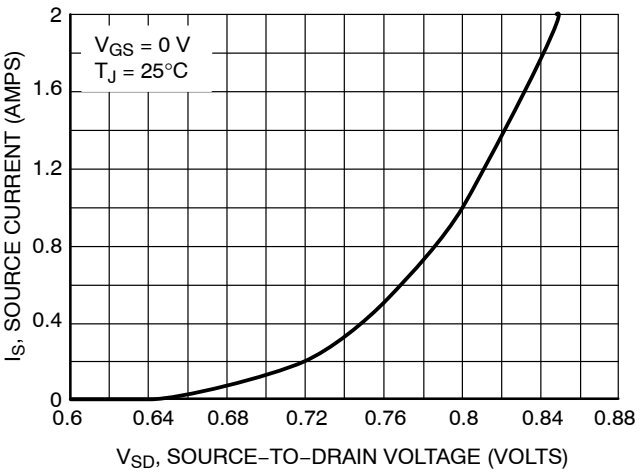


Figure 10. Diode Forward Voltage versus Current

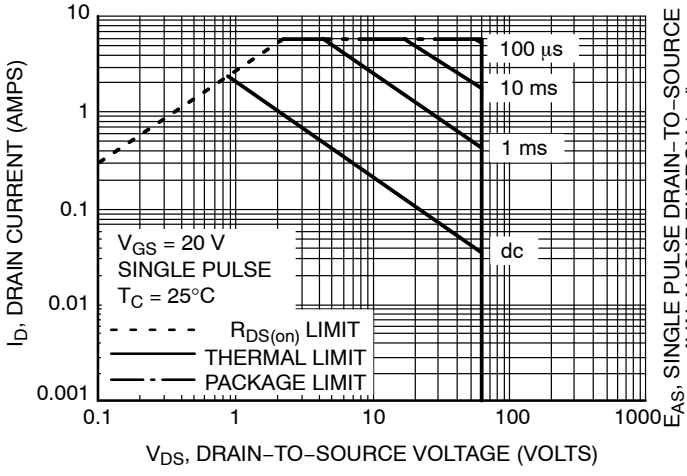


Figure 11. Maximum Rated Forward Biased Safe Operating Area

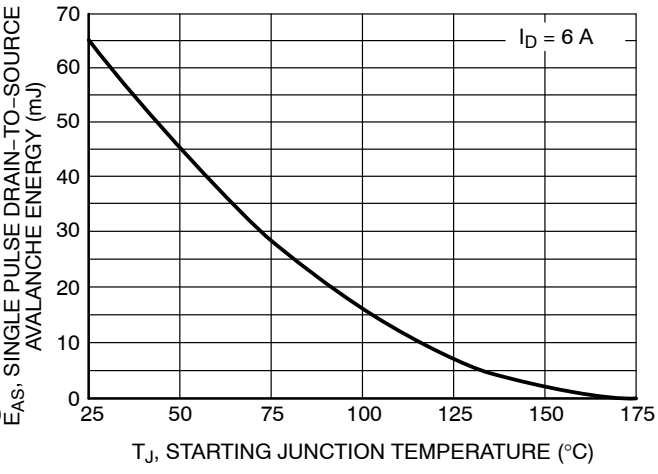


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

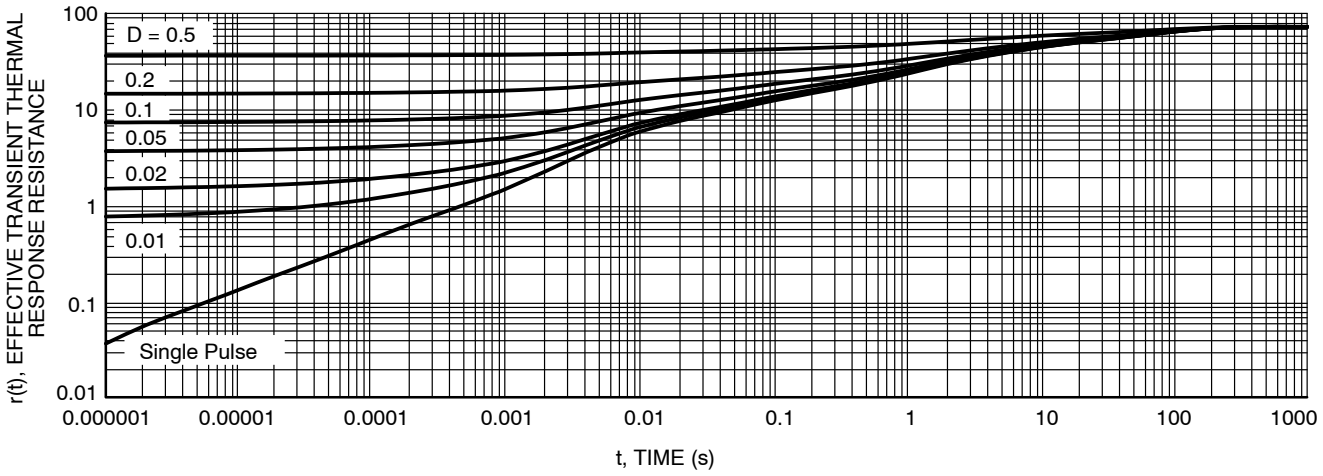


Figure 13. Thermal Response

ORDERING INFORMATION

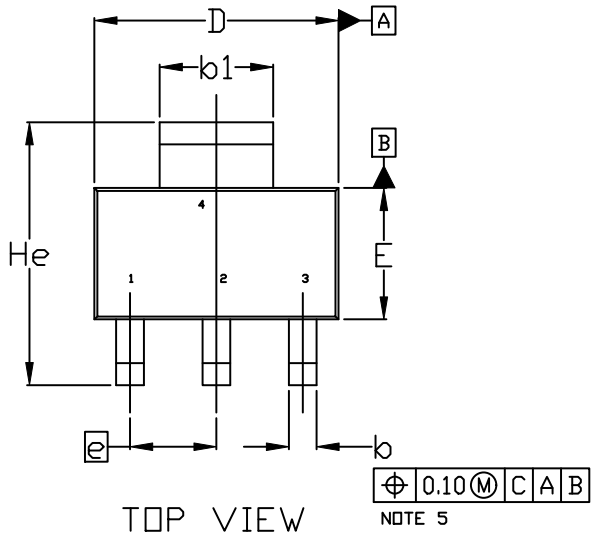
Device	Package	Shipping†
NTF3055L175T1G	SOT−223 (TO−261) (Pb−Free)	1000 / Tape & Reel

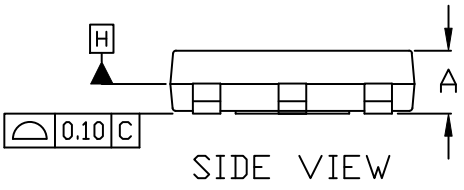
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

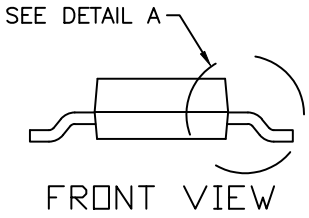
SCALE 1:1

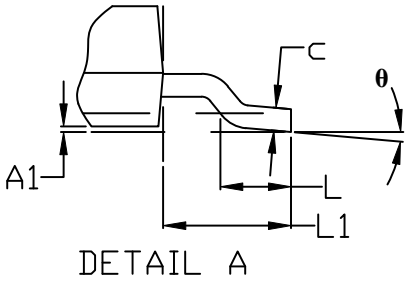
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



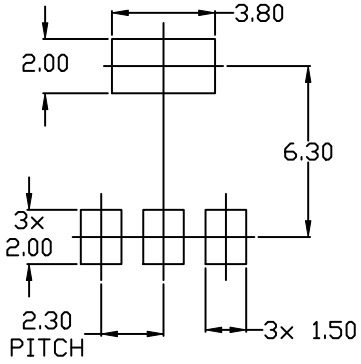






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

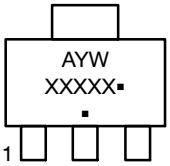
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2

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