# **MOSFET** – Power, N-Channel, DPAK/IPAK 68 A, 30 V

#### **Features**

- Ultra Low R<sub>DS(on)</sub>
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I<sub>DSS</sub> Specified at Elevated Temperature
- DPAK Mounting Information Provided
- These Devices are Pb-Free and are RoHS Compliant

#### **Applications**

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery Powered Products: i.e., Computers, Printers, Cellular and Cordless Telephones, and PCMCIA Cards

#### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	30	Vdc
Gate-to-Source Voltage - Continuous	V <sub>GS</sub>	±20	Vdc
Thermal Resistance – Junction–to–Case Total Power Dissipation @ $T_C$ = 25°C Continuous Drain Current @ $T_C$ = 25°C (Note 4) Continuous Drain Current @ $T_C$ = 100°C	$\begin{array}{c} R_{\thetaJC} \\ P_{D} \\ I_{D} \\ I_{D} \end{array}$	1.65 75 68 43	°C/W W A A
Thermal Resistance – Junction–to–Ambient (Note 2) Total Power Dissipation @ $T_A$ = 25°C Continuous Drain Current @ $T_A$ = 25°C Continuous Drain Current @ $T_A$ = 100°C Pulsed Drain Current (Note 3)	R <sub>θJA</sub> P <sub>D</sub> I <sub>D</sub> I <sub>DM</sub>	67 1.87 11.3 7.1 36	°C/W W A A A
Thermal Resistance – Junction–to–Ambient (Note 1) Total Power Dissipation @ T <sub>A</sub> = 25°C Continuous Drain Current @ T <sub>A</sub> = 25°C Continuous Drain Current @ T <sub>A</sub> = 100°C Pulsed Drain Current (Note 3)	R <sub>θJA</sub> P <sub>D</sub> I <sub>D</sub> I <sub>DM</sub>	120 1.04 8.4 5.3 28	°C/W W A A A
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ( $V_{DD}$ = 30 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 17 Apk, $L$ = 5.0 mH, $R_G$ = 25 $\Omega$ )	E <sub>AS</sub>	722	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

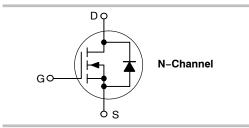
- 1. When surface mounted to an FR4 board using the minimum recommended pad size. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.
- 3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
- 4. Current Limited by Internal Lead Wires.



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V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
30 V	7.8 mΩ @ 10 V	68 A



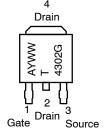


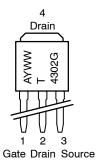




**IPAK** CASE 369D (Straight Lead) STYLE 2

#### MARKING DIAGRAMS **& PIN ASSIGNMENTS**





= Assembly Location\* = Year

WW = Work Week T4302 = Device Code = Pb-Free Package G

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Char	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage		V <sub>(BR)DSS</sub>	30			Vdc
$(V_{GS} = 0 \text{ Vdc}, I_D = 250 \mu\text{A})$ Positive Temperature Coefficient			-	25	-	mV/°C
Zero Gate Voltage Drain Current						μAdc
$(V_{GS} = 0 \text{ Vdc}, V_{DS} = 30 \text{ Vdc}, T_J = 0 \text{ Vdc}, V_{DS} = 30 \text{ Vdc}, T_J = 0 \text{ Vdc}, V_{DS} = 30 \text{ Vdc}, T_J = 0 \text{ Vdc}, T_J = 0 \text{ Vdc}, V_{DS} = 30 \text{ Vdc}, T_J = 0 \text{ Vdc}, V_{DS} = 30 \text{ Vdc}, T_J = 0 \text{ Vdc}, V_{DS} = 30 \text{ Vdc}, T_J = 0 $			_	_	1.0 10	
(V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 30 Vdc, T <sub>J</sub> =			_	_		n A do
Gate-Body Leakage Current (V <sub>GS</sub> = DN CHARACTERISTICS	= ±20 vac, v <sub>DS</sub> = 0 vac)	I <sub>GSS</sub>	_	_	±100	nAdc
Gate Threshold Voltage		V <sub>GS(th)</sub>				Vdc
$(V_{DS} = V_{GS}, I_D = 250 \mu Adc)$		VGS(th)	1.0	1.9	3.0	Vac
Negative Temperature Coefficient			-	-3.8	1	
Static Drain-Source On-State Resi	stance	R <sub>DS(on)</sub>				Ω
$(V_{GS} = 10 \text{ Vdc}, I_D = 20 \text{ Adc})$ $(V_{GS} = 10 \text{ Vdc}, I_D = 10 \text{ Adc})$			_	0.0078 0.0078	0.010 0.010	
$(V_{GS} = 10 \text{ Vdc}, I_D = 10 \text{ Adc})$ $(V_{GS} = 4.5 \text{ Vdc}, I_D = 5.0 \text{ Adc})$			_	0.0078	0.010	
Forward Transconductance (V <sub>DS</sub> =	15 Vdc, I <sub>D</sub> = 10 Adc)	gFS	_	20	_	Mhos
YNAMIC CHARACTERISTICS			•			
Input Capacitance		C <sub>iss</sub>	-	2050	2400	pF
Output Capacitance	$(V_{DS} = 24 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, f = 1.0 \text{ MHz})$	C <sub>oss</sub>	-	640	800	
Reverse Transfer Capacitance	1 = 1.0 NH 12)	C <sub>rss</sub>	-	225	310	
WITCHING CHARACTERISTICS (N	lote 6)					
Turn-On Delay Time		t <sub>d(on)</sub>	-	11	20	ns
Rise Time	$(V_{DD} = 25 \text{ Vdc}, I_D = 1.0 \text{ Adc},$	t <sub>r</sub>	-	15	25	
Turn-Off Delay Time	$V_{GS} = 10 \text{ Vdc},$ $R_G = 6.0 \Omega)$	t <sub>d(off)</sub>	-	85	130	
Fall Time	ζ ,	t <sub>f</sub>	-	55	90	
Turn-On Delay Time		t <sub>d(on)</sub>	-	11	20	ns
Rise Time	$(V_{DD} = 25 \text{ Vdc}, I_D = 1.0 \text{ Adc}, V_{GS} = 10 \text{ Vdc},$	t <sub>r</sub>	_	13	20	
Turn-Off Delay Time	$R_{G} = 10 \text{ VdC},$ $R_{G} = 2.5 \Omega)$	t <sub>d(off)</sub>	-	55	90	
Fall Time		t <sub>f</sub>	_	40	75	
Turn-On Delay Time		t <sub>d(on)</sub>	-	15	1	ns
Rise Time	$(V_{DD} = 24 \text{ Vdc}, I_D = 20 \text{ Adc}, V_{GS} = 10 \text{ Vdc},$	t <sub>r</sub>	-	25	ı	
Turn-Off Delay Time	$V_{GS} = 10 \text{ VdC},$ $R_{G} = 2.5 \Omega)$	t <sub>d(off)</sub>	-	40	ı	
Fall Time	ζ ,	t <sub>f</sub>	-	58	ı	
Gate Charge	04.44.4	$Q_{T}$	-	55	80	nC
	$(V_{DS} = 24 \text{ Vdc}, I_D = 2.0 \text{ Adc}, V_{GS} = 10 \text{ Vdc})$	Q <sub>gs</sub> (Q1)	-	5.5	-	
	- 43 10 140/	Q <sub>gd</sub> (Q2)	_	15	-	
ODY-DRAIN DIODE RATINGS (No	te 5)					
Diode Forward On-Voltage		$V_{SD}$				Vdc
$(I_S = 2.3 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = 20 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = 2.3 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$			_	0.75	1.0	
			_	0.90 0.65	_ _	
Reverse Recovery Time		t <sub>rr</sub>	_	39	65	ns
,	$(I_S = 2.3 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$	t <sub>a</sub>	_	20	_	
	$dI_S/dt = 100 A/\mu s)$	t <sub>b</sub>	_	19	_	
Reverse Recovery Stored Charge				0.043		μС

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Indicates Pulse Test: Pulse Width = 300 µsec max, Duty Cycle ≤ 2%.

<sup>6.</sup> Switching characteristics are independent of operating junction temperature.

#### **TYPICAL CHARACTERISTICS**

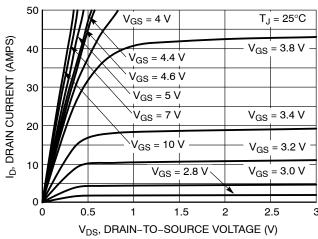


Figure 1. On-Region Characteristics

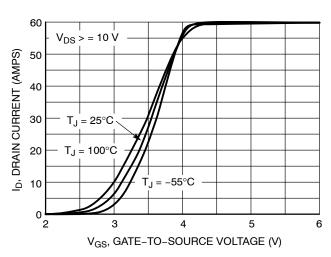


Figure 2. Transfer Characteristics

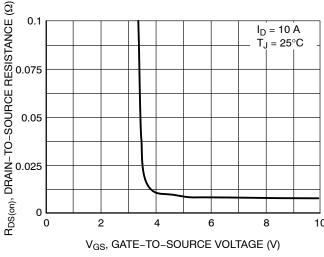


Figure 3. On–Resistance vs. Gate–To–Source Voltage

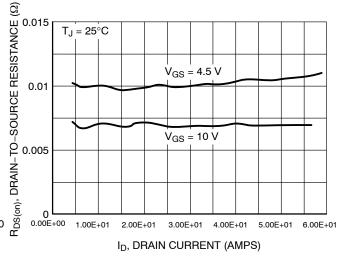


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

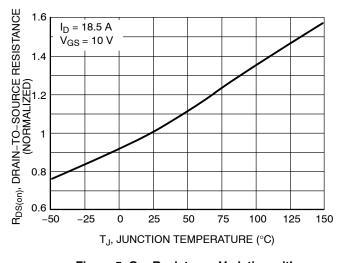


Figure 5. On–Resistance Variation with Temperature

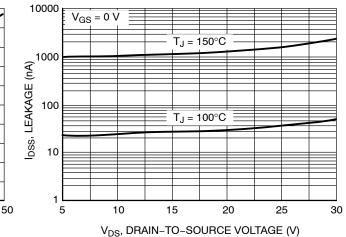


Figure 6. Drain-To-Source Leakage Current vs. Voltage

#### **TYPICAL CHARACTERISTICS**

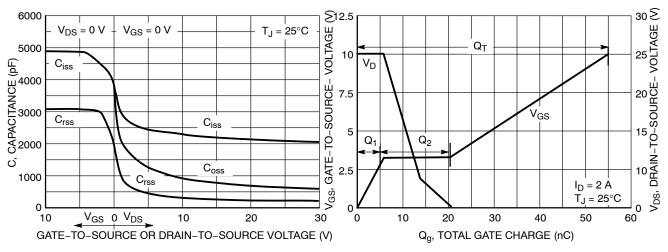


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

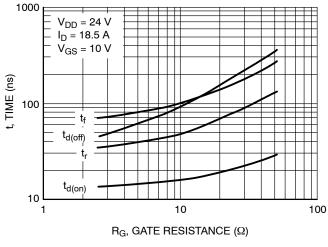


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

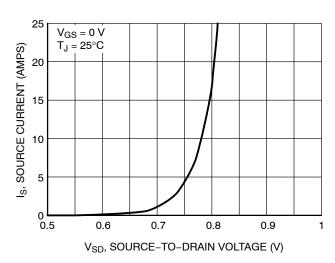
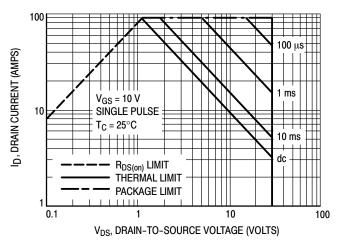


Figure 10. Diode Forward Voltage vs. Current

#### **TYPICAL CHARACTERISTICS**



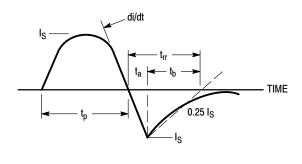


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Diode Reverse Recovery Waveform

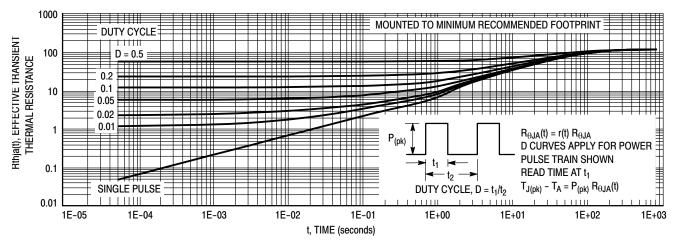


Figure 13. Thermal Response - Various Duty Cycles

#### **ORDERING INFORMATION**

Device	Package Type	Package	Shipping <sup>†</sup>
NTD4302G	DPAK	369C (Pb-Free)	75 Units / Rail
NTD4302-1G	IPAK	369D (Pb-Free)	75 Units / Rail
NTD4302T4G	DPAK	369C (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

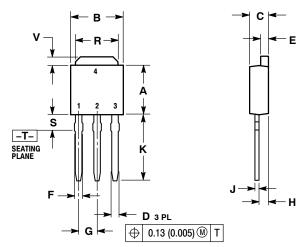


# **DPAK INSERTION MOUNT**

CASE 369 ISSUE O

**DATE 02 JAN 2000** 





- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.250	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090	BSC	2.29 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
٧	0.030	0.050	0.77	1.27

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:		STYLE 5:		STYLE 6:	
PIN 1.	BASE	PIN 1.	GATE	PIN 1.	ANODE	PIN 1.	CATHODE	PIN 1.	GATE	PIN 1.	MT1
2.	COLLECTOR	2.	DRAIN	2.	CATHODE	2.	ANODE	2.	ANODE	2.	MT2
3.	EMITTER	3.	SOURCE	3.	ANODE	3.	GATE	3.	CATHODE	3.	GATE
4.	COLLECTOR	4.	DRAIN	4.	CATHODE	4.	ANODE	4.	ANODE	4.	MT2

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DESCRIPTION:	DPAK INSERTION MOUNT		PAGE 1 OF 1	

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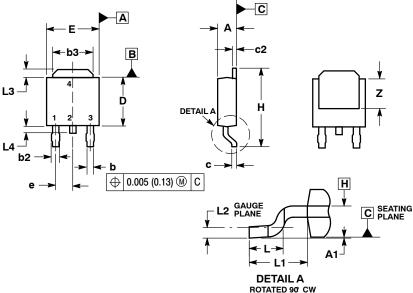
# **DPAK (SINGLE GUAGE)** CASE 369AA **ISSUE B** SCALE 1:1 C

**DATE 03 JUN 2010** 

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCHES.
  3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-
- MENSIONS b3, L3 and Z.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
е	0.090	BSC	2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	



# STYLE 1: PIN 1. BASE

PIN 1. GATE 2. ANODE 3. CATHODE

4. ANODE

STYLE 5:

2. COLLECTOR 3. EMITTER 4. COLLECTOR

# STYLE 2: PIN 1. GATE

2. DRAIN 3. SOURCE 4. DRAIN

## STYLE 3:

PIN 1. ANODE 2. CATHODE 3. ANODE CATHODE

# STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE

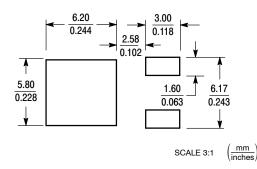
STYLE 7:

## STYLE 6: PIN 1. MT1 2. MT2

3. GATE

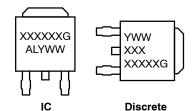
#### PIN 1. GATE 2. COLLECTOR 3. EMITTER COLLECTOR

#### **SOLDERING FOOTPRINT\***



<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### **GENERIC** MARKING DIAGRAM\*



XXXXXX = Device Code Α = Assembly Location L = Wafer Lot ٧ = Year = Work Week WW = Pb-Free Package

DOCUMENT NUMBER:	98AON13126D	Electronic versions are uncontrolled except when accessed directly from the Document Reposi Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1	

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<sup>\*</sup>This information is generic. Please refer to device data sheet for actual part

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