

# MOSFET - Power, N-Channel, SUPERFET® III, FAST

650 V, 49 A, 50 mΩ

## NTBL050N65S3H

### Description

SUPERFET III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFAST III FAST MOSFET series helps minimize various power systems and improve system efficiency. The TOLL package offers improved thermal performance and excellent switching performance thanks to Kelvin Source configuration and lower parasitic source inductance. TOLL offers Moisture Sensitivity Level 1 (MSL 1).

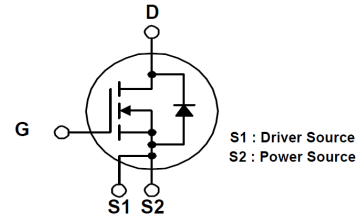
### Features

- 700 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 40\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 98\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 909\text{ pF}$ )
- 100% Avalanche Tested
- Kelvin Source Configuration and Low Parasitic Source Inductance
- MSL1 Qualified
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

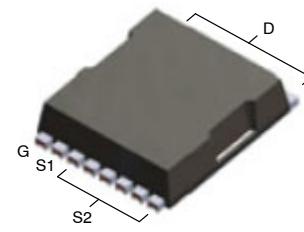
### Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	50 mΩ @ 10 V	49 A

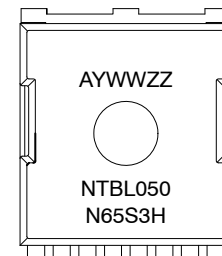


N-Channel MOSFET



H-PSOF8L  
CASE 100DC

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- NTBL050N65S3H = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NTBL050N65S3H

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C, Unless otherwise specified)

Symbol	Parameter	Value	Unit
V <sub>DSS</sub>	Drain to Source Voltage	650	V
V <sub>GSS</sub>	Gate to Source Voltage	DC	±30
		AC (f > 1 Hz)	±30
I <sub>D</sub>	Drain Current	Continuous (T <sub>C</sub> = 25°C)	49
		Continuous (T <sub>C</sub> = 100°C)	31
I <sub>DM</sub>	Drain Current	Pulsed (Note 1)	132
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	491	mJ
I <sub>AS</sub>	Avalanche Current (Note 2)	6.8	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	3.05	mJ
dv/dt	MOSFET dv/dt	120	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	305
		Derate Above 25°C	2.44
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I<sub>AS</sub> = 6.8 A, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 24.5 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ 400 V, starting T<sub>J</sub> = 25°C.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case, Steady State	0.41	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, Steady State (Note 4)	43	

4. Device on 1 in<sup>2</sup>, 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
NTBL050N65S3H	NTBL050N65S3H	H-PSOF8L	13" mm	24 mm	2000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NTBL050N65S3H

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	650	–	–	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 150°C	700	–	–	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C	–	0.63	–	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V	–	–	1.0	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C	–	3.21	–	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 4.8 mA	2.4	–	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 24.5 A	–	42.5	50	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 24.5 A	–	52	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	4880	–	pF
C <sub>oss</sub>	Output Capacitance		–	70	–	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	909	–	pF
C <sub>oss(er.)</sub>	Energy Related Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	128	–	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 24.5 A, V <sub>GS</sub> = 10 V (Note 5)	–	98	–	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		–	24	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge		–	25	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.6	–	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 24.5 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 4.7 Ω (Note 5)	–	32	–	ns
t <sub>r</sub>	Turn-On Rise Time		–	9.5	–	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	96	–	ns
t <sub>f</sub>	Turn-Off Fall Time		–	2.6	–	ns

### SOURCE-DRAIN DIODE CHARACTERISTICS

I <sub>S</sub>	Maximum Continuous Source to Drain Diode Forward Current	–	–	49	A	
I <sub>SM</sub>	Maximum Pulsed Source to Drain Diode Forward Current	–	–	132	A	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 24.5 A	–	–	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 24.5 A, dI <sub>F</sub> /dt = 100 A/μs	–	442	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	8.8	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

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## TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

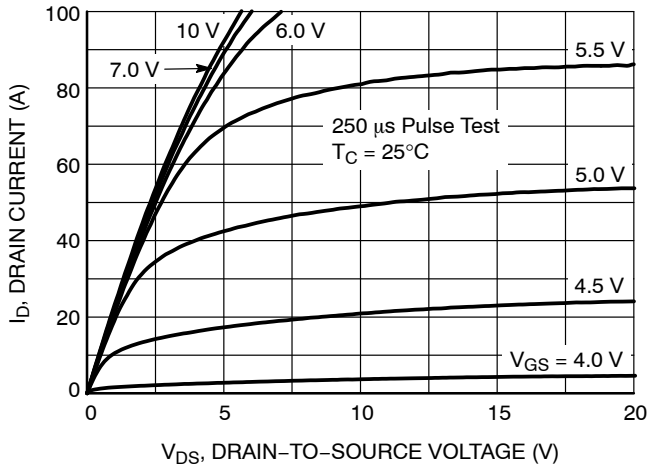


Figure 1. On-Region Characteristics

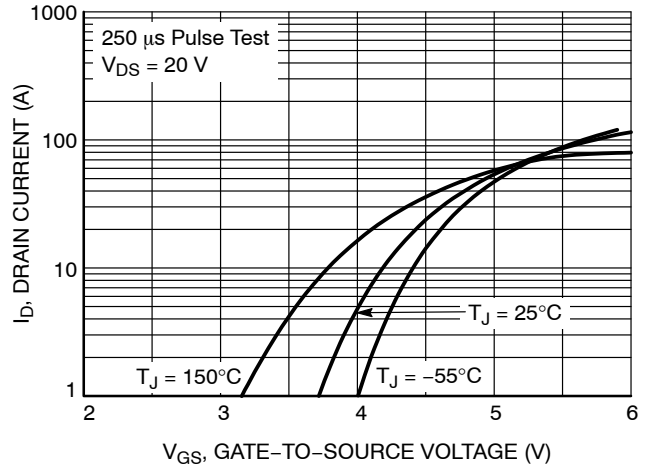


Figure 2. Transfer Characteristics

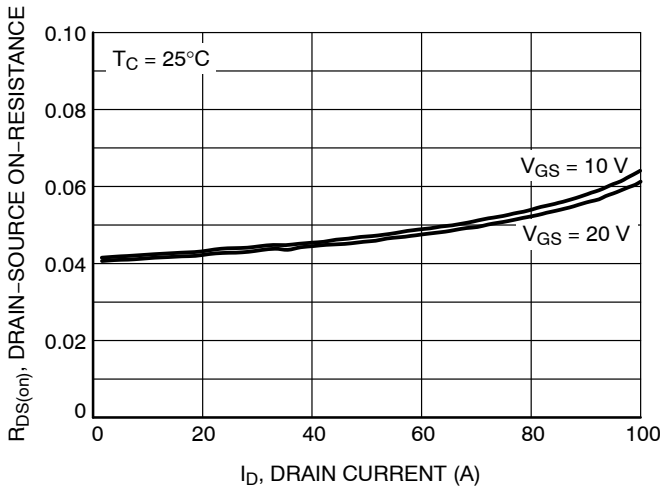


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

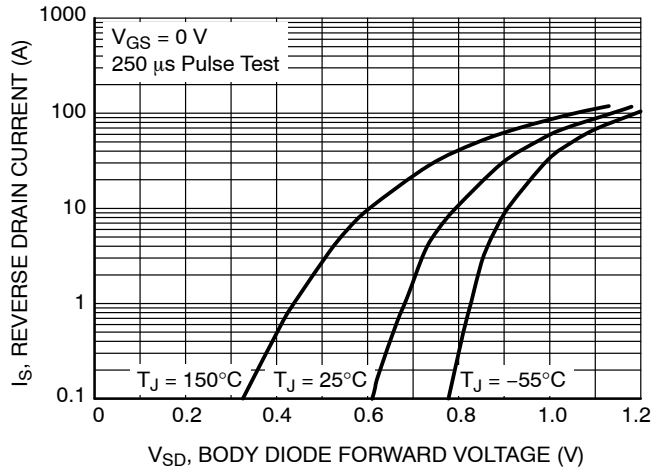


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

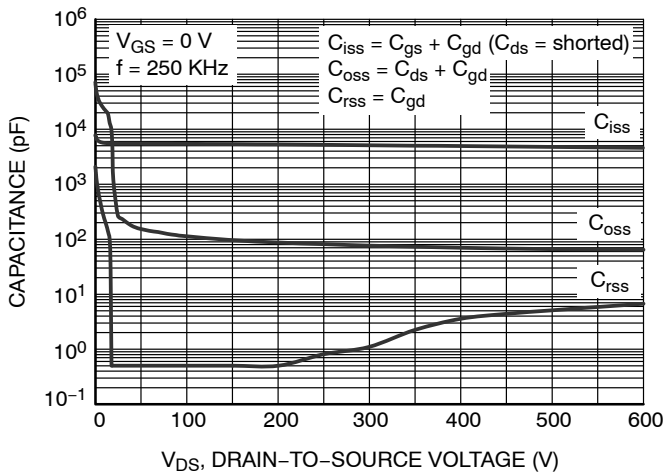


Figure 5. Capacitance Characteristics

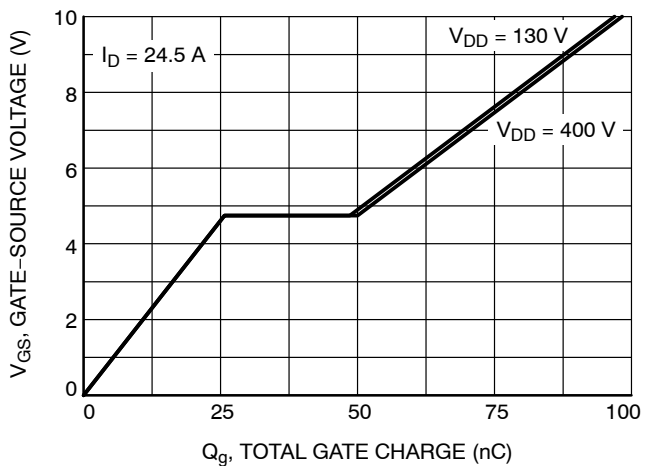
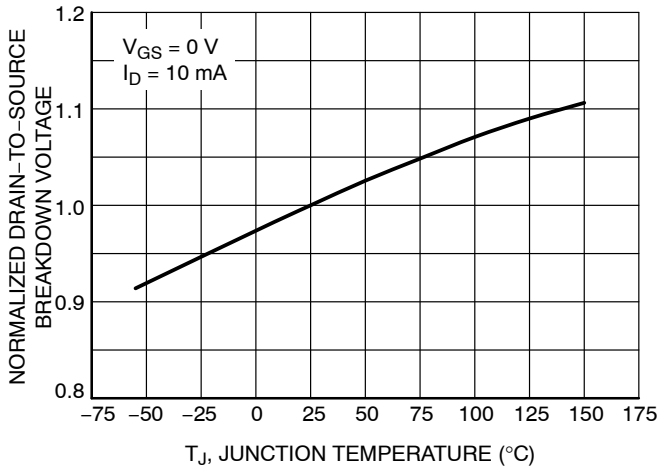


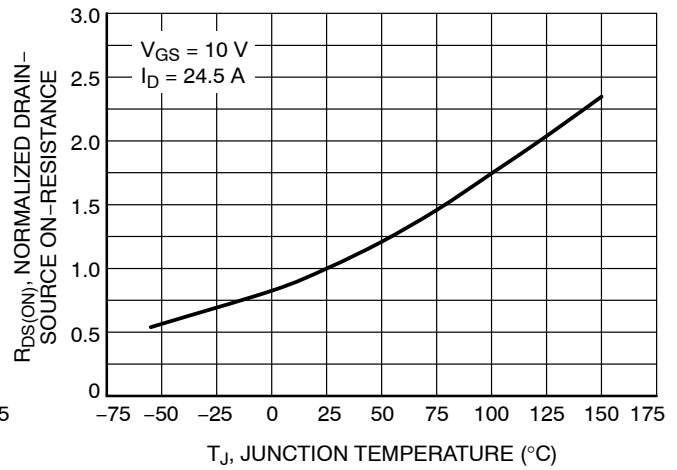
Figure 6. Gate Charge Characteristics

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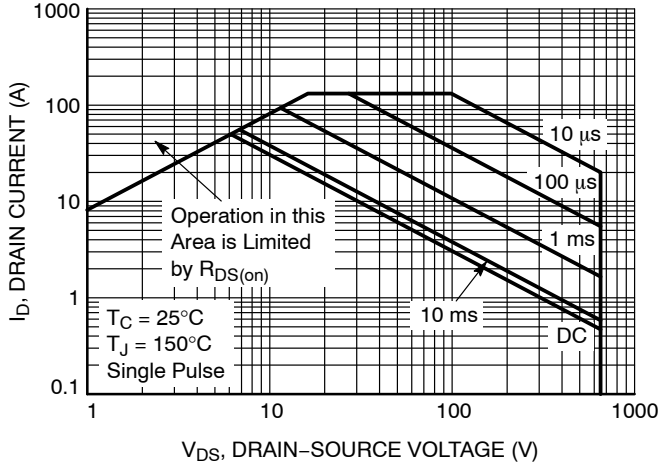
## TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



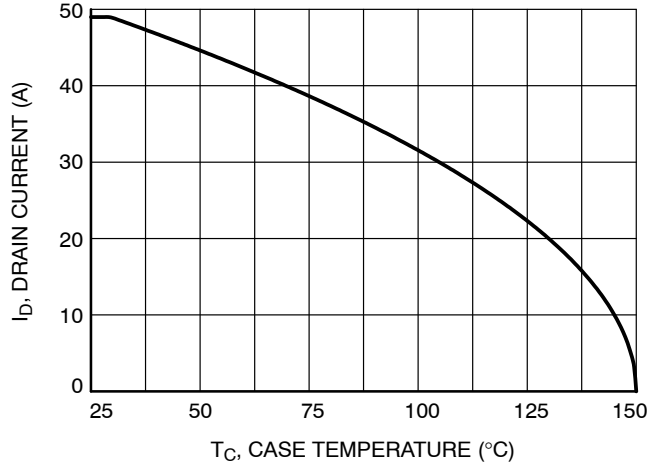
**Figure 7. Breakdown Voltage Variation vs. Temperature**



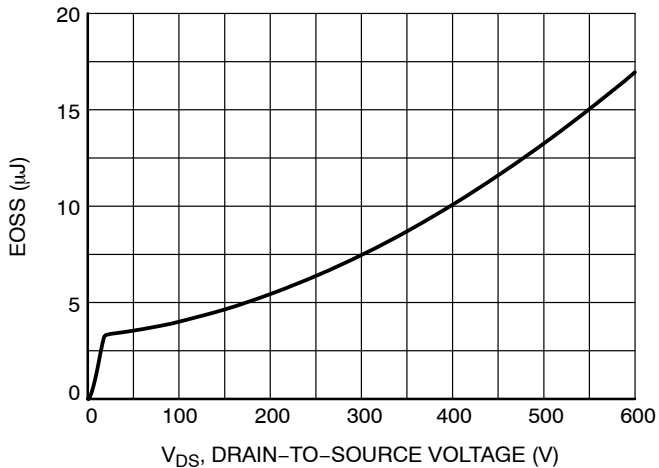
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



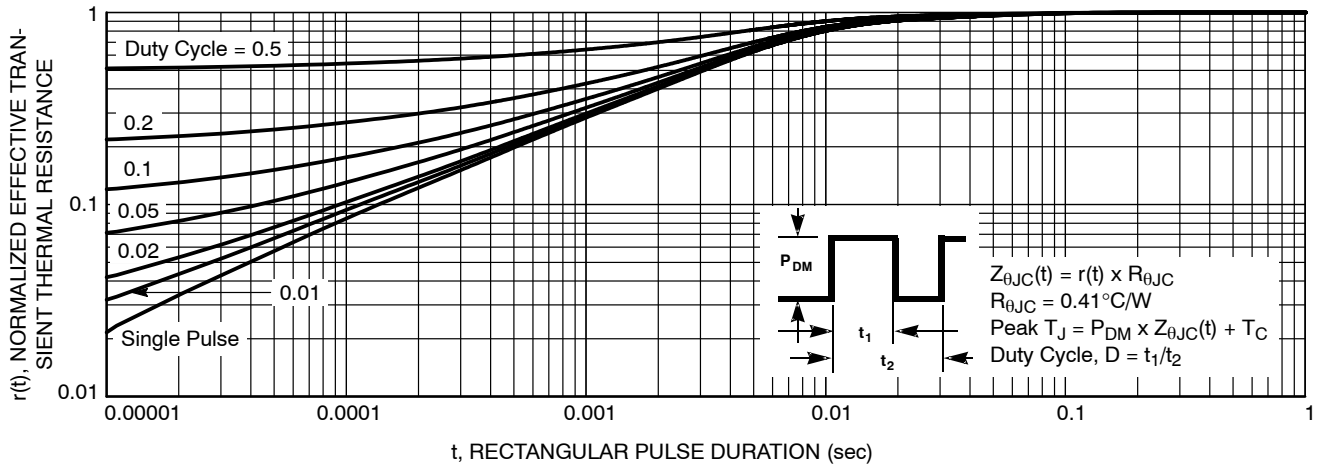
**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11.  $E_{OSS}$  vs. Drain to Source Voltage**

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## TYPICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



**Figure 12. Transient Thermal Impedance**

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Figure 13. Gate Charge Test Circuit & Waveform

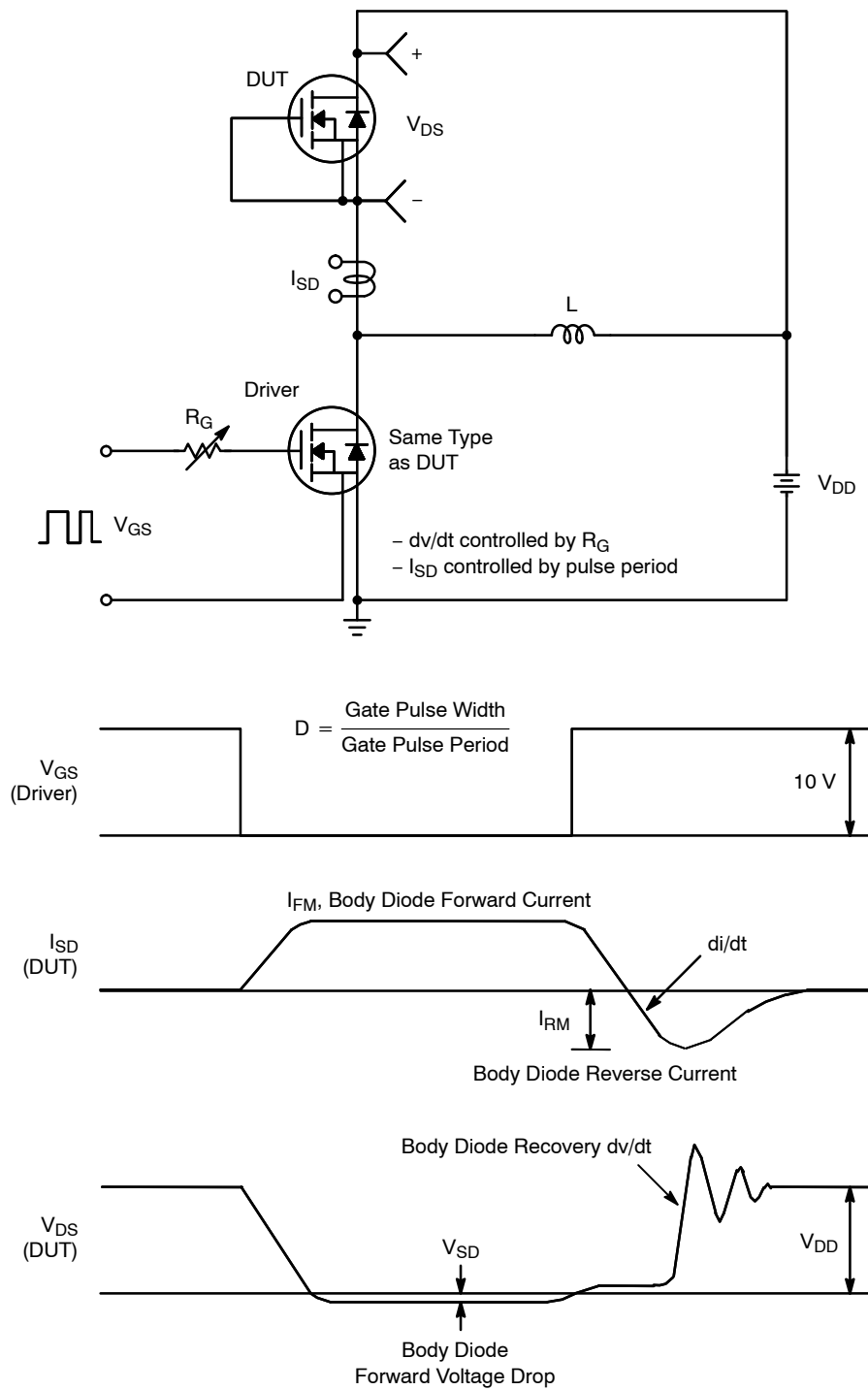


Figure 14. Resistive Switching Test Circuit & Waveforms



Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

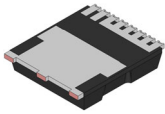
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**Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

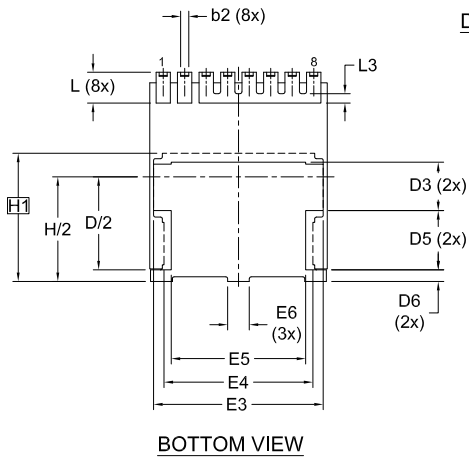
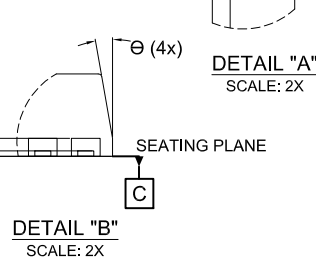
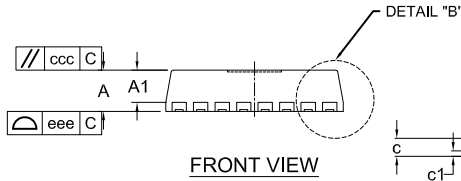
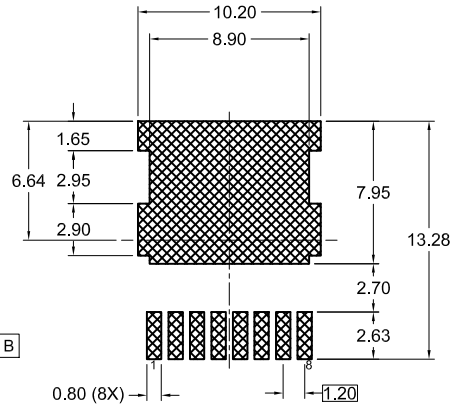
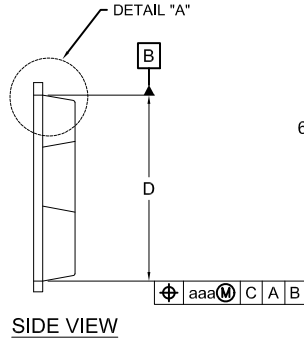
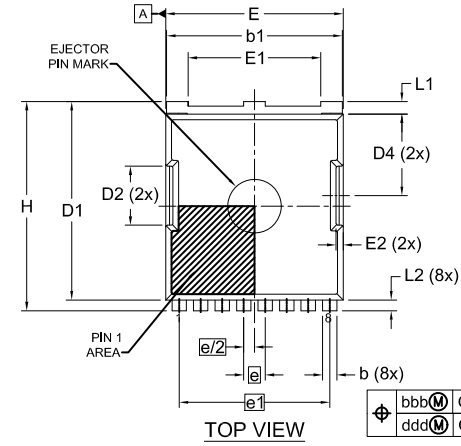


# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

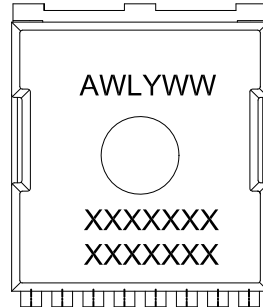


**H-PSOF8L 9.90x11.68, 1.20P**  
CASE 100DC  
ISSUE A

DATE 18 MAY 2023



### GENERIC MARKING DIAGRAM\*



A = ASSY LOCATION  
WL = WAFER LOT CODE  
Y = YEAR CODE  
WW = WORK WEEK CODE  
XXXXXXXX = DEVICE CODE  
XXXXXXXX = DEVICE CODE

\*THIS INFORMATION IS GENERIC.  
PLEASE REFER TO DEVICE DATA SHEET FOR ACTUAL PART MARKING.

- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  3. CONTROLLING DIMENSION: MILLIMETERS.
  4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
  5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	---	---
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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