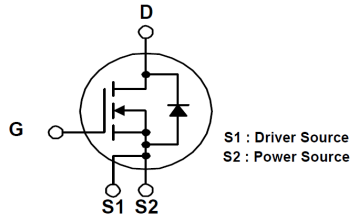
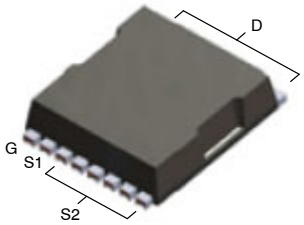
MOSFET - Power, N-Channel, SUPERFET® III, FAST
650 V, 49 A, 50 mΩ

NTBL050N65S3H

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
650 V	50 mΩ @ 10 V	49 A



N−Channel MOSFET



H−PSOF8L
CASE 100DC

Description

SUPERFET III MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFAST III FAST MOSFET series helps minimize various power systems and improve system efficiency. The TOLL package offers improved thermal performance and excellent switching performance thanks to Kelvin Source configuration and lower parasitic source inductance. TOLL offers Moisture Sensitivity Level 1 (MSL 1).

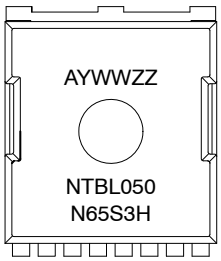
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 40 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 98 nC)
- Low Effective Output Capacitance (Typ. $_{Coss(eff.)}$ = 909 pF)
- 100% Avalanche Tested
- Kelvin Source Configuration and Low Parasitic Source Inductance
- MSL1 Qualified
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Assembly Lot Code
NTBL050N65S3H	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	49	A
		Continuous (T_C = 100°C)	31	
I_{DM}	Drain Current	Pulsed (Note 1)	132	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		491	mJ
I_{AS}	Avalanche Current (Note 2)		6.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		3.05	mJ
dv/dt	MOSFET dv/dt		120	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	305	W
		Derate Above 25°C	2.44	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 s		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 6.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 24.5 A, di/dt ≤ 100 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Steady State	0.41	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Steady State (Note 4)	43	

4. Device on 1 in^2, 2 oz copper pad on 1.5 x 1.5 in. board of FR−4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
NTBL050N65S3H	NTBL050N65S3H	H−PSOF8L	13” mm	24 mm	2000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	0.63	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	1.0	μA
		V_{DS} = 520 V, T_C = 125°C	–	3.21	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 4.8 mA	2.4	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 24.5 A	–	42.5	50	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 24.5 A	–	52	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	4880	–	pF
C_{oss}	Output Capacitance		–	70	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	909	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	128	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 24.5 A, V_{GS} = 10 V (Note 5)	–	98	–	nC
Q_{gs}	Gate to Source Gate Charge		–	24	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	25	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.6	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 24.5 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 5)	–	32	–	ns
t_r	Turn-On Rise Time		–	9.5	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	96	–	ns
t_f	Turn-Off Fall Time		–	2.6	–	ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	49	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	132	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 24.5 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 24.5 A, dI_F/dt = 100 A/μs	–	442	–	ns
Q_{rr}	Reverse Recovery Charge		–	8.8	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

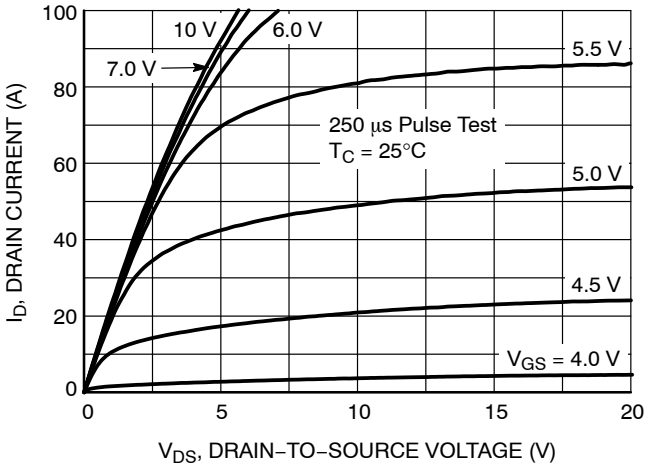


Figure 1. On−Region Characteristics

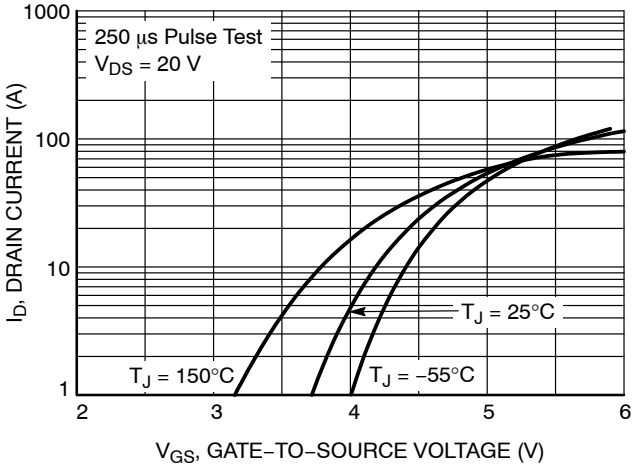


Figure 2. Transfer Characteristics

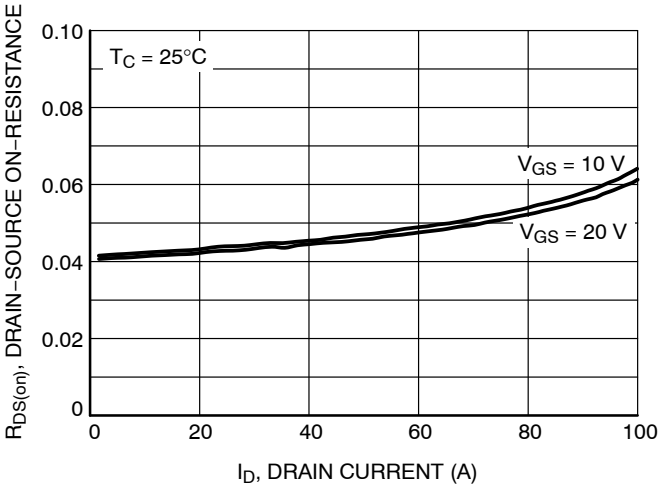


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

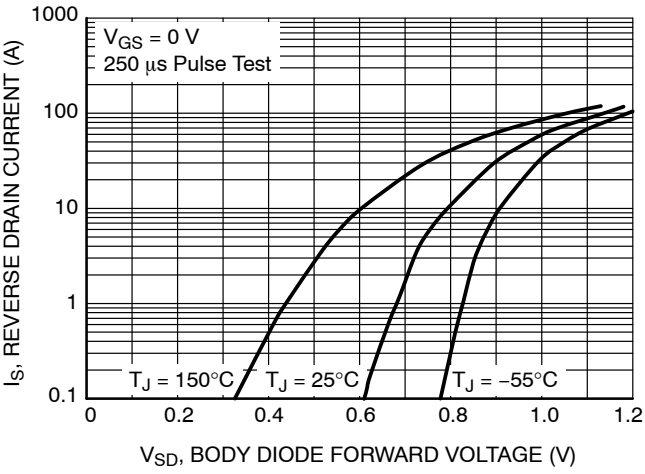


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

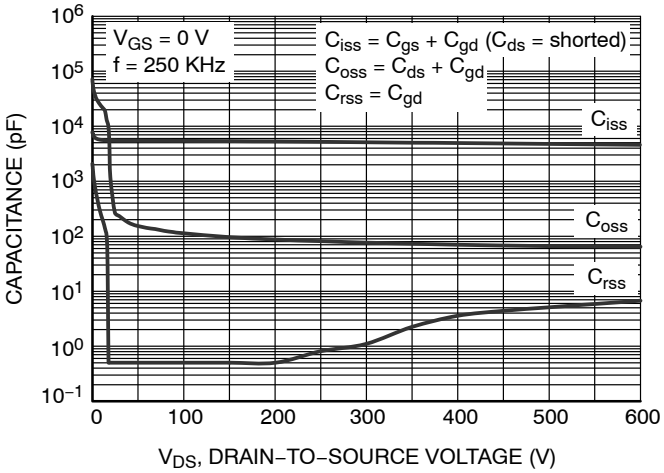


Figure 5. Capacitance Characteristics

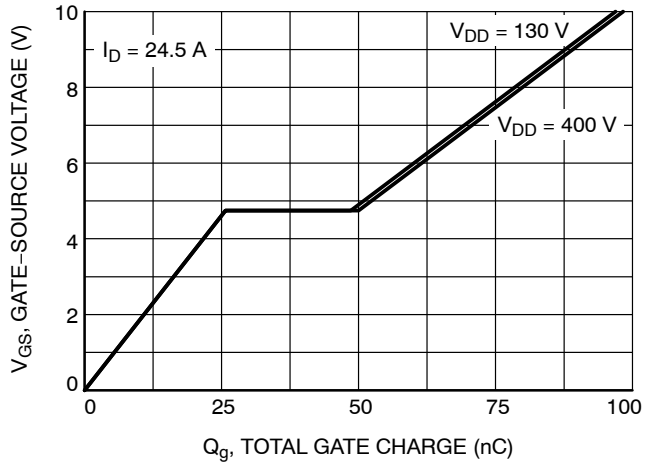


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

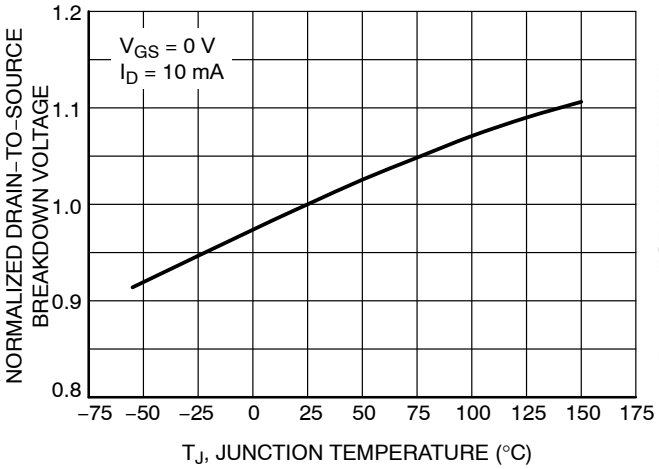


Figure 7. Breakdown Voltage Variation vs. Temperature

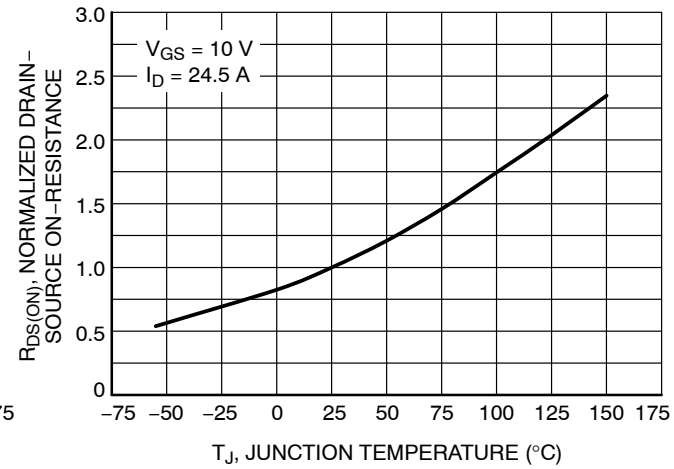


Figure 8. On−Resistance Variation vs. Temperature

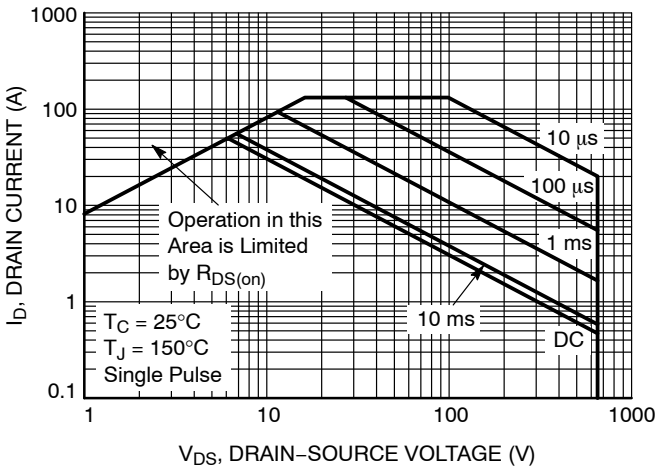


Figure 9. Maximum Safe Operating Area

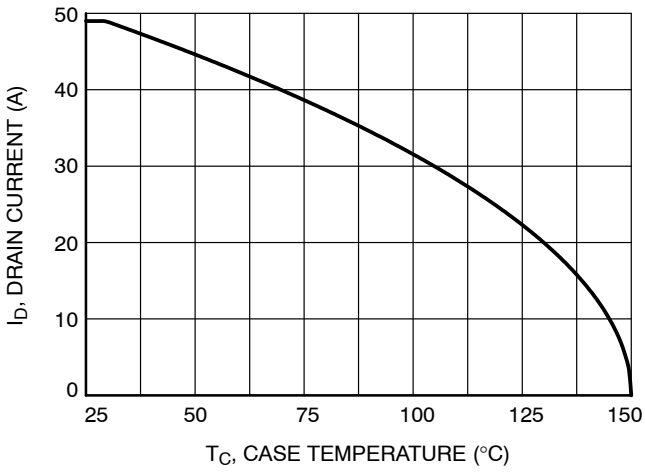


Figure 10. Maximum Drain Current vs. Case Temperature

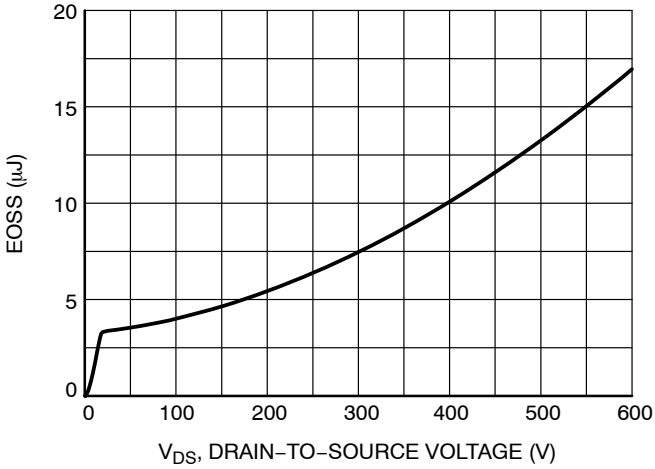


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (T_C = 25°C UNLESS OTHERWISE NOTED)

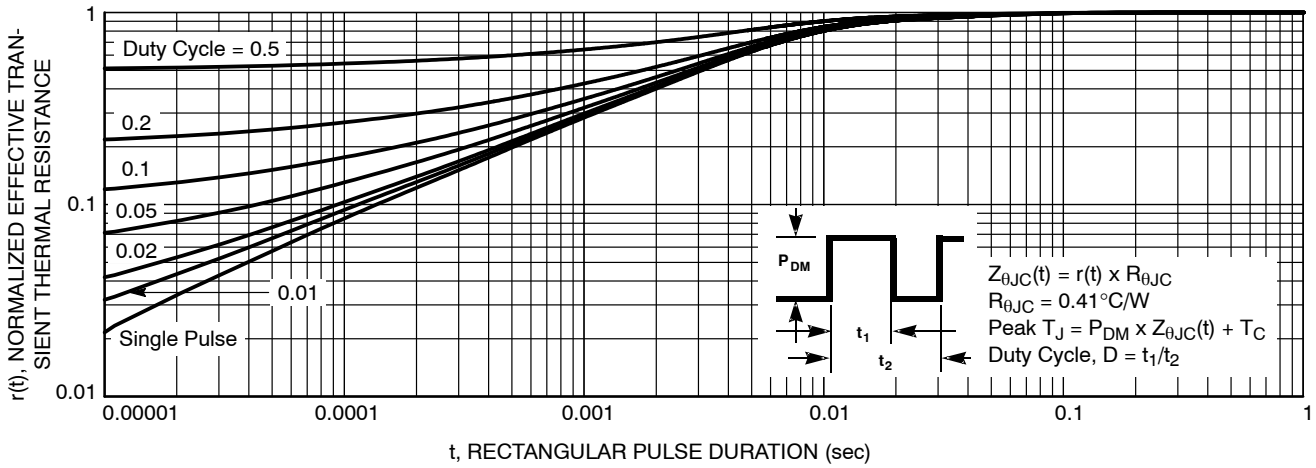


Figure 12. Transient Thermal Impedance

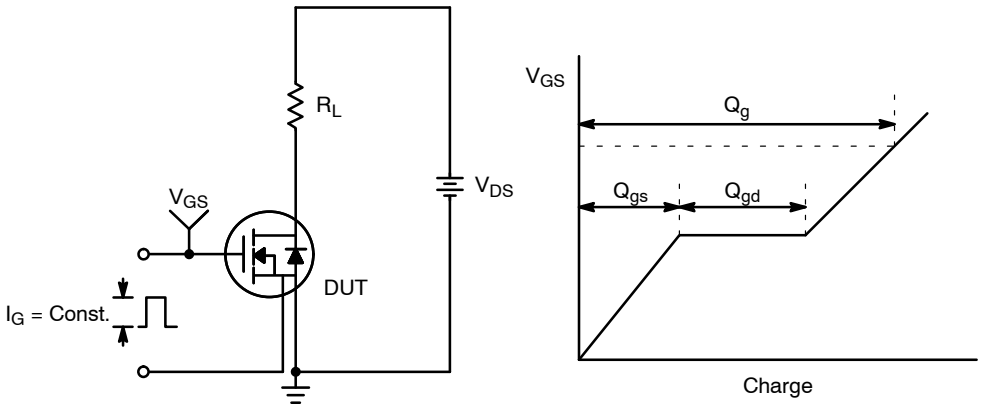


Figure 13. Gate Charge Test Circuit & Waveform

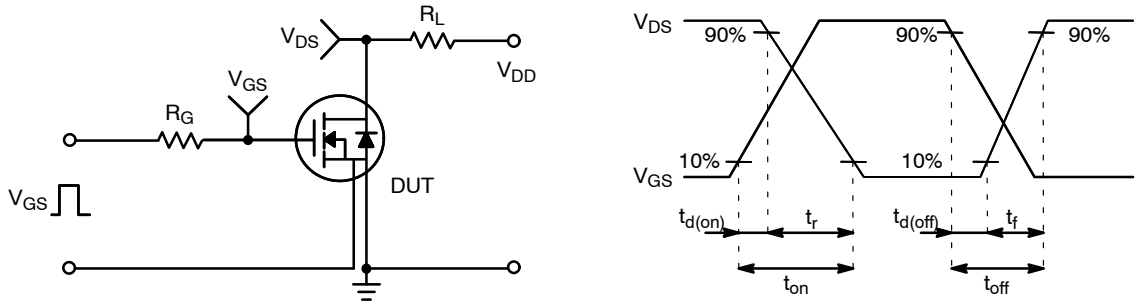


Figure 14. Resistive Switching Test Circuit & Waveforms

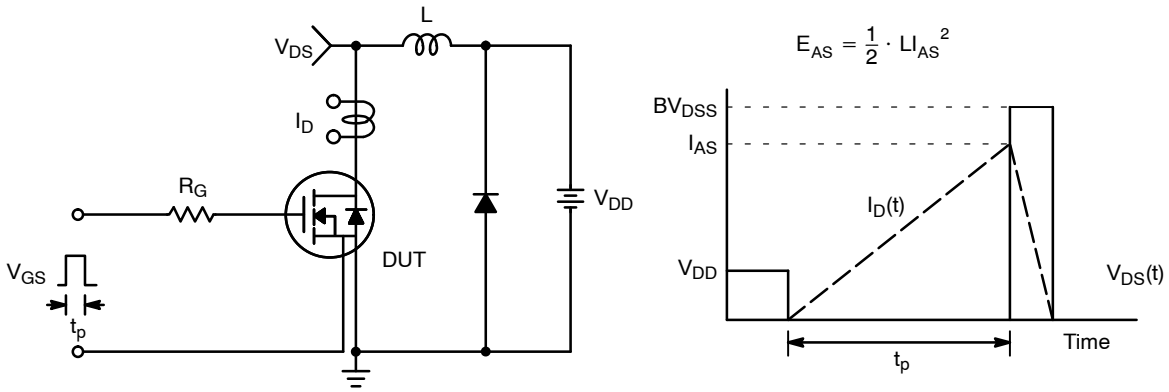


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

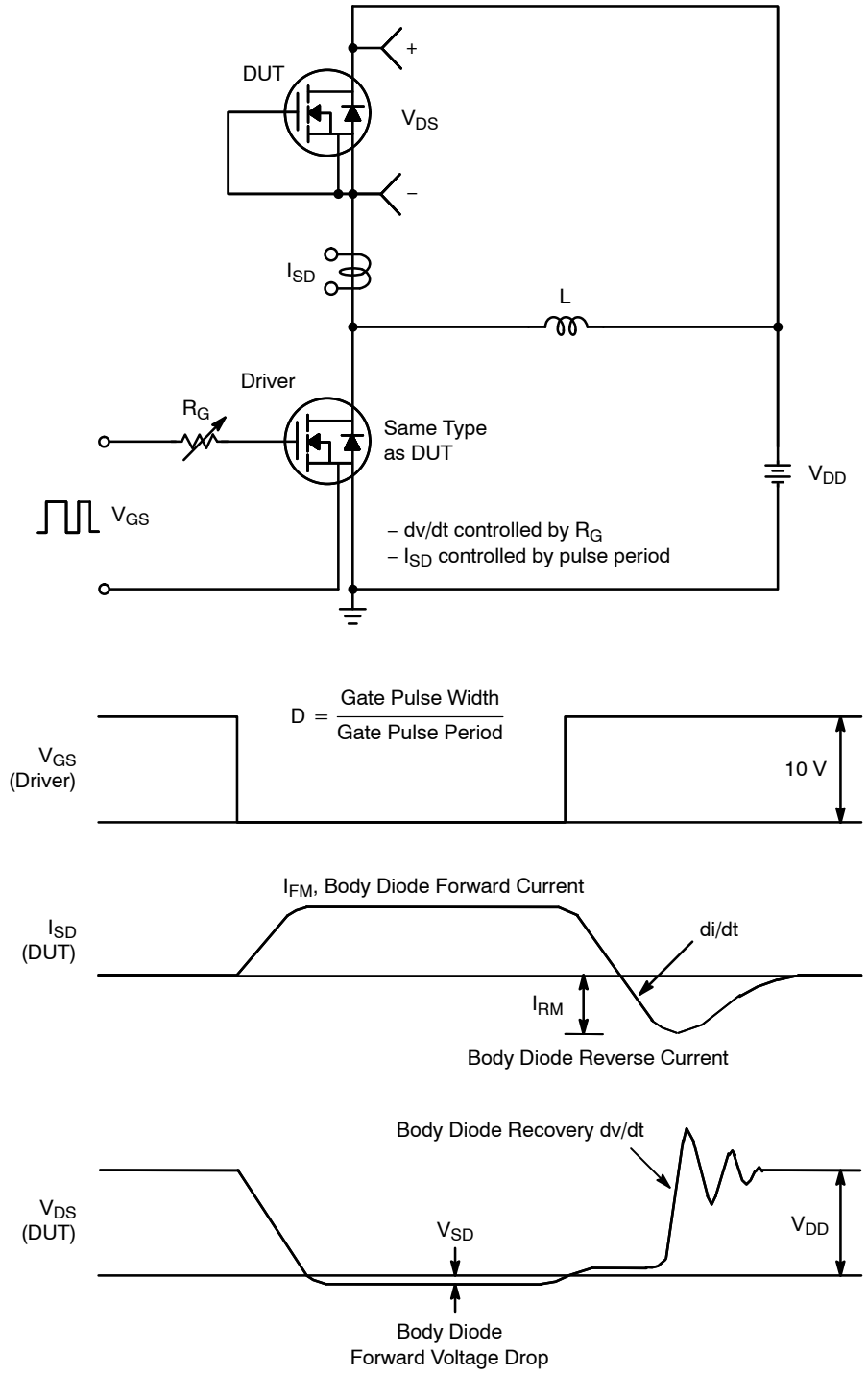
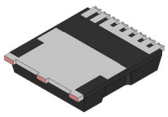


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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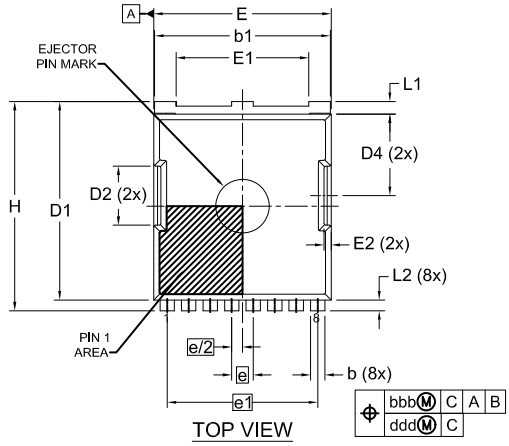
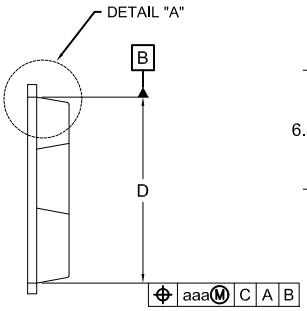
ISSUE A

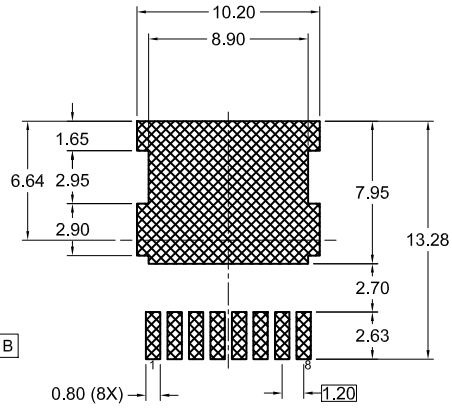
DATE 18 MAY 2023



TOP VIEW

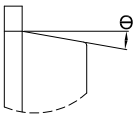


SIDE VIEW

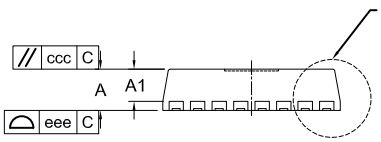


LAND PATTERN RECOMMENDATION

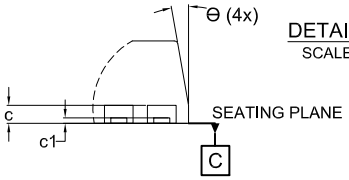
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL "A"
SCALE: 2X



FRONT VIEW



DETAIL "B"
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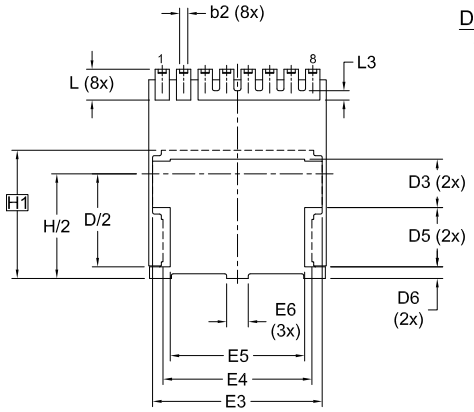
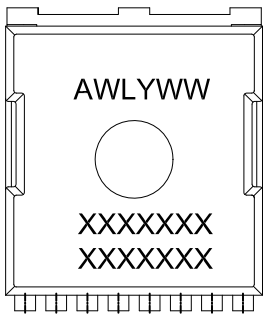


BOTTOM VIEW

GENERIC MARKING DIAGRAM*



A = ASSY LOCATION
WL = WAFER LOT CODE
Y = YEAR CODE
WW = WORK WEEK CODE
XXXXXXX = DEVICE CODE
XXXXXXX = DEVICE CODE

*THIS INFORMATION IS GENERIC. PLEASE REFER TO DEVICE DATA SHEET FOR ACTUAL PART MARKING.

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	---	---
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e		1.20 BSC	
e/2		0.60 BSC	
e1		8.40 BSC	
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1		7.15 BSC	
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
θ	0°	---	12°
aaa		0.20	
bbb		0.25	
ccc		0.20	
ddd		0.20	
eee		0.10	

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DESCRIPTION:	**H−PSOF8L 9.90x11.68, 1.20P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales