Bipolar Transistor -160 V, -1 A, Low V_{CE}(sat), PNP Single

NSVT1418L

This device is bipolar junction transistor featuring high current, low saturation voltage, and high speed switching.

Suitable for automotive applications. AEC−Q101 qualified and PPAP capable.

Features

- Large Current Capacitance
- Low Collector to Emitter Saturation Voltage
- High Speed Switching
- High Allowable Power Dissipation
- AEC−Q101 Qualified and PPAP Capable
- Pb−Free, Halogen Free and RoHS Compliant
- Ultra Small Package Facilitates Miniaturization in End Products

Typical Applications

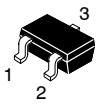
- High Side Switch
- Lighting, Infotainment

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Parameter	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	−180	V
Collector to Emitter Voltage	V_{CEO}	−160	V
Emitter to Base Voltage	V_{EBO}	−6	V
Collector Current	I_C	−1	A
Collector Current (Pulse)	I_{CP}	−2	A
Collector Dissipation (Note 1)	P_C	0.42	W
Junction Temperature	Tj	150	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on ceramic substrate. (250 mm^2 x 0.8 mm)



SOT−23
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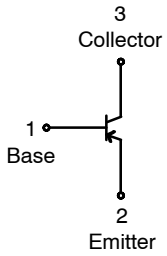
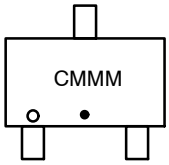
ELECTRICAL CONNECTION



MARKING DIAGRAM



CMM = Specific Device Code
M = Single Digit Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Collector Cutoff Current	I_{CBO}	V_{CB} = −120 V, I_E = 0 A			−0.1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = −4 V, I_C = 0 A			−0.1	μA
DC Current Gain	h_{FE1}	V_{CE} = −5 V, I_C = −100 mA	100		400	
	h_{FE2}	V_{CE} = −5 V, I_C = −10 mA	90			
Gain−Bandwidth Product	f_T	V_{CE} = −10 V, I_C = −50 mA		120		MHz
Output Capacitance	Cob	V_{CB} = −10 V, f = 1 MHz		11		pF
Collector to Emitter Saturation Voltage	V_{CE}(sat)1	I_C = −250 mA, I_B = −25 mA		−0.1	−0.5	V
	V_{CE}(sat)2	I_C = −250 mA, I_B = −50 mA		−0.08	−0.13	V
Base to Emitter Saturation Voltage	V_{BE}(sat)	I_C = −250 mA, I_B = −25 mA		−0.8	−1.2	V
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = −10 μA, I_E = 0 A	−180			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = −1 mA, R_{BE} = ∞	−160			V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = −10 μA, I_C = 0 A	−6			V
Turn−On Time	t_{on}	See Figure 1		90		ns
Storage Time	t_{stg}			1000		ns
Fall Time	t_f			70		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

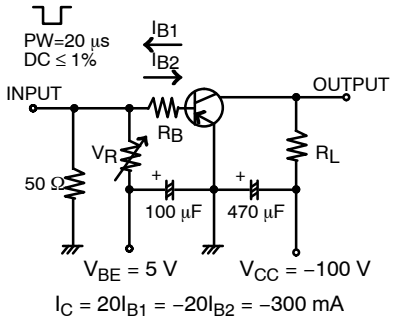


Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTICS

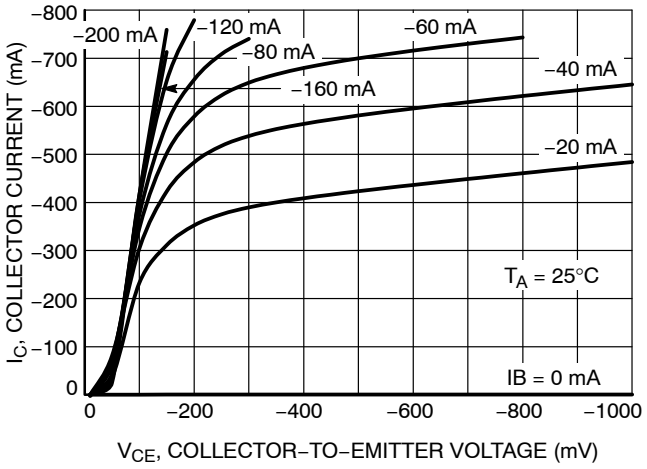


Figure 2. I_C vs. V_{CE}

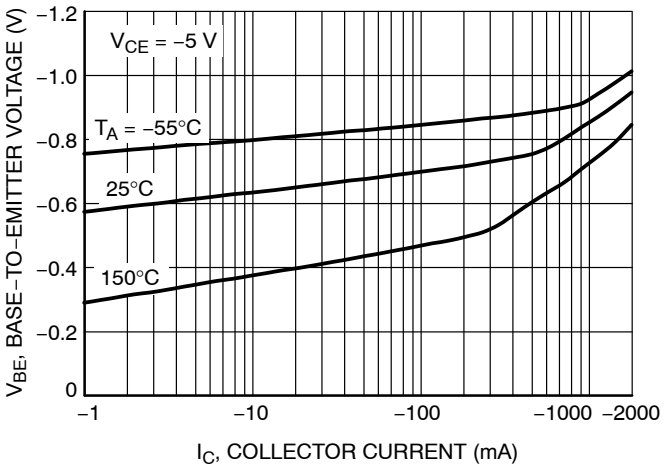


Figure 3. V_{BE} vs. I_C

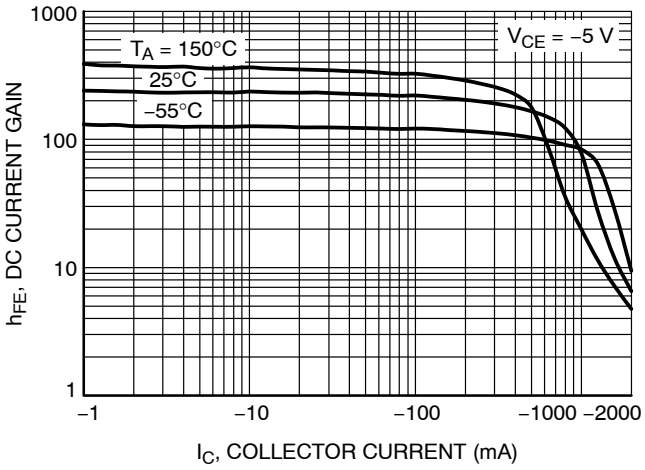


Figure 4. h_{FE} vs. I_C

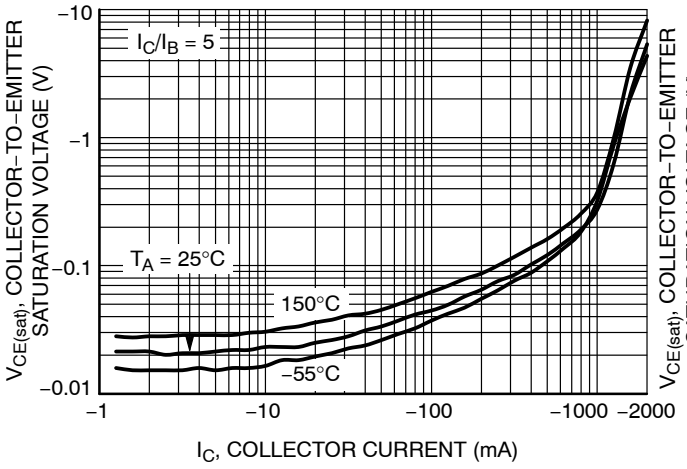


Figure 5. $V_{CE(sat)}$ vs. I_C

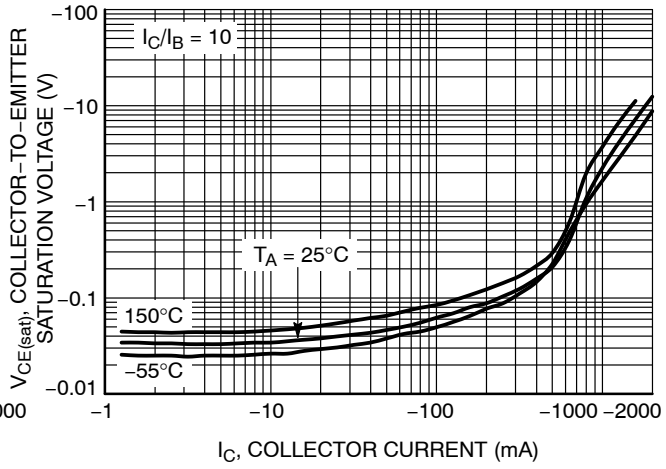


Figure 6. $V_{CE(sat)}$ vs. I_C

TYPICAL CHARACTERISTICS

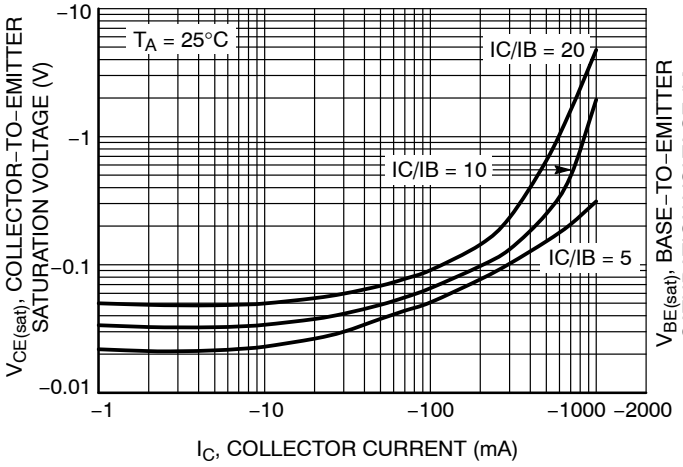


Figure 7. $V_{CE(sat)}$ vs. I_C

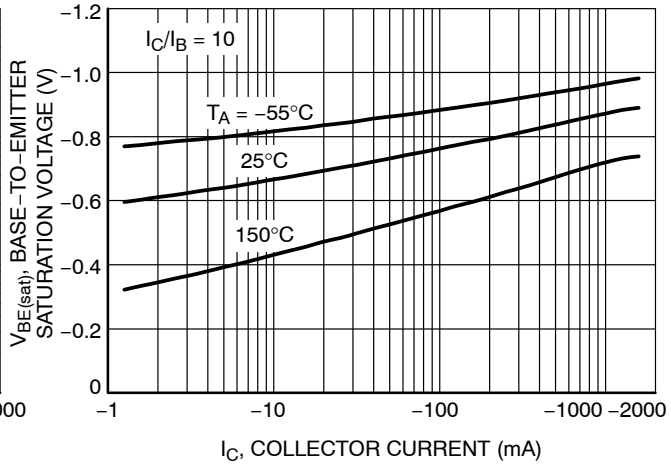


Figure 8. $V_{BE(sat)}$ vs. I_C

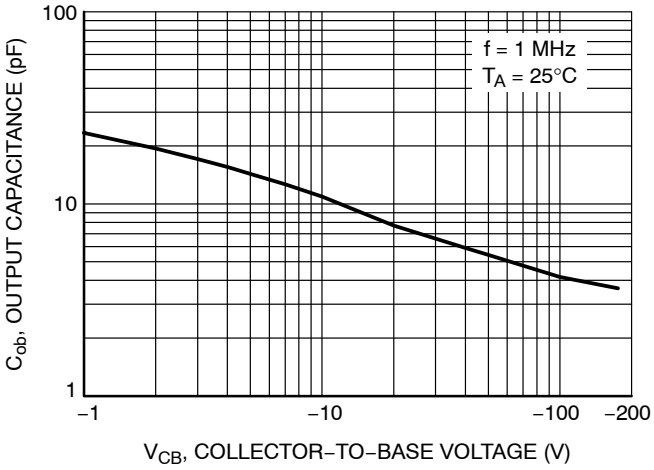


Figure 9. C_{ob} vs. V_{CB}

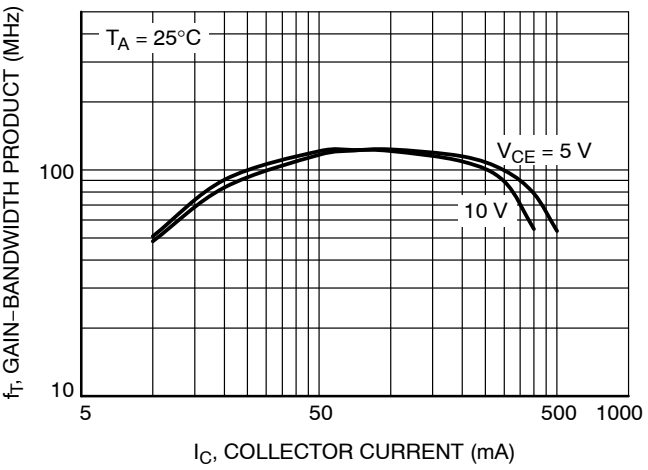


Figure 10. f_T vs. I_C

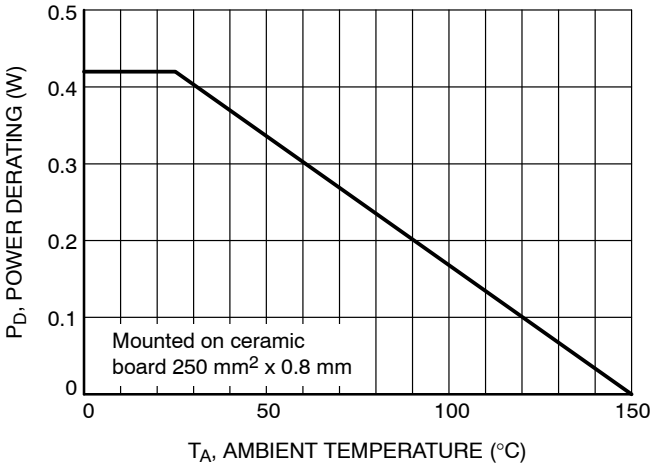


Figure 11. Power Derating

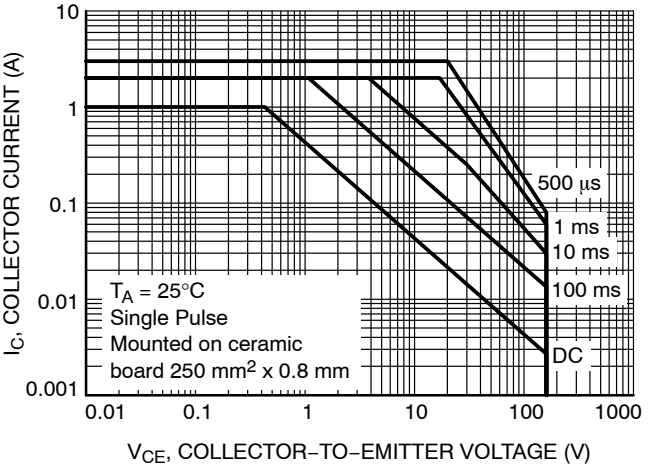


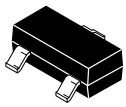
Figure 12. Safe Operating Area

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing) †
NSVT1418LT1G	CMM	SOT−23 (Pb−Free / Halogen Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

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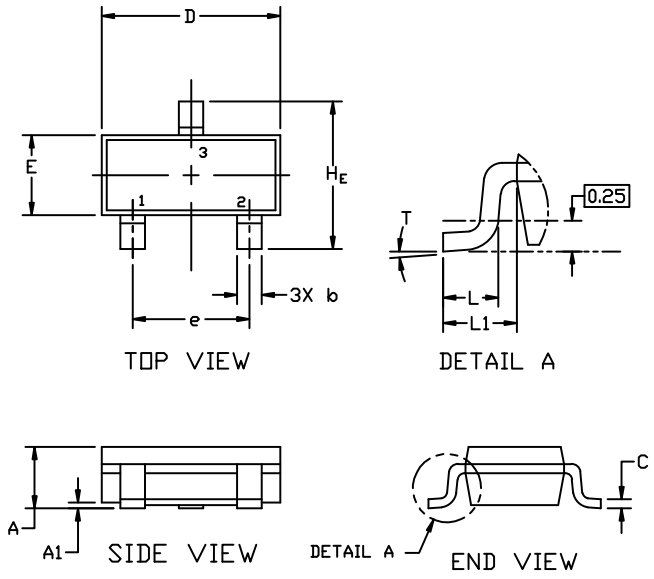
DATE 01 MAR 2023

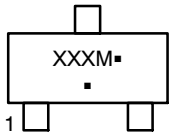


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

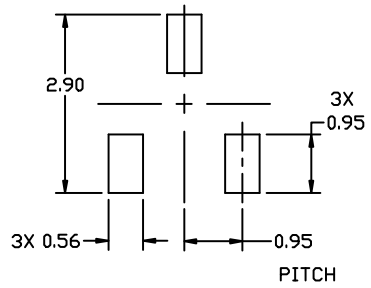
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

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STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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