

NSTB1002DXV5T1G, NSTB1002DXV5T5G

Preferred Devices

Dual Common Base-Collector Bias Resistor Transistors NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSTB1002DXV5T1G series, two complementary devices are housed in the SOT-553 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- These are Pb-Free Devices

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q₁ and Q₂, - minus sign for Q₁ (PNP) omitted)

| Rating | Symbol | Value | | Unit |
|---------------------------|-----------|-------|-----|------|
| | | Q1 | Q2 | |
| Collector-Base Voltage | V_{CBO} | -40 | 50 | Vdc |
| Collector-Emitter Voltage | V_{CEO} | -40 | 50 | Vdc |
| Collector Current | I_C | -200 | 100 | mAdc |

THERMAL CHARACTERISTICS

| Characteristic (One Junction Heated) | Symbol | Max | Unit |
|--|-----------------|------------------------------|----------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 357 (Note 1) 2.9 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance – Junction-to-Ambient | $R_{\theta JA}$ | 350 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Characteristic (Both Junctions Heated) | Symbol | Max | Unit |
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 500 (Note 1) 4.0 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance – Junction-to-Ambient | $R_{\theta JA}$ | 250 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

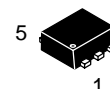
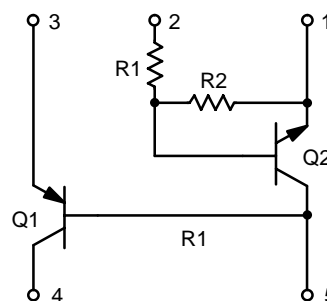
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-4 @ Minimum Pad



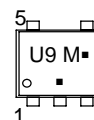
ON Semiconductor®

<http://onsemi.com>



SOT-553
CASE 463B

MARKING DIAGRAM



U9 = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping |
|-----------------|----------------------|--------------------------------|
| NSTB1002DXV5T1G | SOT-553 (Pb-Free) | 4 mm pitch 4000/Tape & Reel |
| NSTB1002DXV5T5G | SOT-553 (Pb-Free) | 2 mm pitch 8000/Tape & Reel |

Preferred devices are recommended choices for future use and best overall value.

NSTB1002DXV5T1G, NSTB1002DXV5T5G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Q1 TRANSISTOR: PNP OFF CHARACTERISTICS

| | | | | | |
|--|----------------------|------|---|-----|------|
| Collector-Emitter Breakdown Voltage (Note 2) | V _{(BR)CEO} | -40 | - | - | Vdc |
| Collector-Base Breakdown Voltage | V _{(BR)CBO} | -40 | - | - | Vdc |
| Emitter-Base Breakdown Voltage | V _{(BR)EBO} | -5.0 | - | - | Vdc |
| Base Cutoff Current | I _{BL} | - | - | -50 | nAdc |
| Collector Cutoff Current | I _{CEX} | - | - | -50 | nAdc |

ON CHARACTERISTICS (Note 2)

| | | | | | |
|---|----------------------|--|-----------------------------|-------------------------|-----|
| DC Current Gain (I _C = -0.1 mAdc, V _{CE} = -1.0 Vdc) (I _C = -1.0 mAdc, V _{CE} = -1.0 Vdc) (I _C = -10 mAdc, V _{CE} = -1.0 Vdc) (I _C = -50 mAdc, V _{CE} = -1.0 Vdc) (I _C = -100 mAdc, V _{CE} = -1.0 Vdc) | h _{FE} | | 60 80 100 60 30 | - - 300 - - | - |
| Collector-Emitter Saturation Voltage (I _C = -10 mAdc, I _B = -1.0 mAdc) (I _C = -50 mAdc, I _B = -5.0 mAdc) | V _{CE(sat)} | | - - | -0.25 -0.4 | Vdc |
| Base-Emitter Saturation Voltage (I _C = -10 mAdc, I _B = -1.0 mAdc) (I _C = -50 mAdc, I _B = -5.0 mAdc) | V _{BE(sat)} | | -0.65 - | -0.85 -0.95 | Vdc |

SMALL-SIGNAL CHARACTERISTICS

| | | | | | |
|--|------------------|-----|------|---|--------------------|
| Current-Gain – Bandwidth Product | f _T | 250 | - | - | MHz |
| Output Capacitance | C _{obo} | - | 4.5 | - | pF |
| Input Capacitance | C _{ibo} | - | 10.0 | - | pF |
| Input Impedance (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{ie} | 2.0 | 12 | - | kΩ |
| Voltage Feedback Ratio (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{re} | 0.1 | 10 | - | X 10 ⁻⁴ |
| Small-Signal Current Gain (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{fe} | 100 | 400 | - | - |
| Output Admittance (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{oe} | 3.0 | 60 | - | μmhos |
| Noise Figure (V _{CE} = -5.0 Vdc, I _C = -100 μAdc, R _S = 1.0 kΩ, f = 1.0 kHz) | nF | - | 4.0 | - | dB |

SWITCHING CHARACTERISTICS

| | | | | | |
|--------------|--|----------------|---|-----|----|
| Delay Time | (V _{CC} = -3.0 Vdc, V _{BE} = 0.5 Vdc) | t _d | - | 35 | ns |
| Rise Time | (I _C = -10 mAdc, I _{B1} = -1.0 mAdc) | t _r | - | 35 | |
| Storage Time | (V _{CC} = -3.0 Vdc, I _C = -10 mAdc) | t _s | - | 225 | ns |
| Fall Time | (I _{B1} = I _{B2} = -1.0 mAdc) | t _f | - | 75 | |

Q2 TRANSISTOR: NPN

OFF CHARACTERISTICS

| | | | | | |
|--|------------------|---|---|-----|------|
| Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0) | I _{CBO} | - | - | 100 | nAdc |
| Collector-Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0) | I _{CEO} | - | - | 500 | nAdc |
| Emitter-Base Cutoff Current (V _{EB} = 6.0, I _C = 5.0 mA) | I _{EBO} | - | - | 0.1 | mAdc |

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

NSTB1002DXV5T1G, NSTB1002DXV5T5G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------|-----|-----|------|------------------|
| ON CHARACTERISTICS | | | | | |
| Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{A}$, $I_E = 0$) | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector-Emitter Breakdown Voltage ($I_C = 2.0 \text{ mA}$, $I_B = 0$) | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| DC Current Gain ($V_{CE} = 10 \text{ V}$, $I_C = 5.0 \text{ mA}$) | h_{FE} | 80 | 140 | – | |
| Collector-Emitter Saturation Voltage ($I_C = 10 \text{ mA}$, $I_B = 0.3 \text{ mA}$) | $V_{CE(SAT)}$ | – | – | 0.25 | Vdc |
| Output Voltage (on) ($V_{CC} = 5.0 \text{ V}$, $V_B = 2.5 \text{ V}$, $R_L = 1.0 \text{ k}\Omega$) | V_{OL} | – | – | 0.2 | Vdc |
| Output Voltage (off) ($V_{CC} = 5.0 \text{ V}$, $V_B = 0.5 \text{ V}$, $R_L = 1.0 \text{ k}\Omega$) | V_{OH} | 4.9 | – | – | Vdc |
| Input Resistor | R1 | 33 | 47 | 61 | $\text{k}\Omega$ |
| Resistor Ratio | R1/R2 | 0.8 | 1.0 | 1.2 | |

2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2.0\%$.

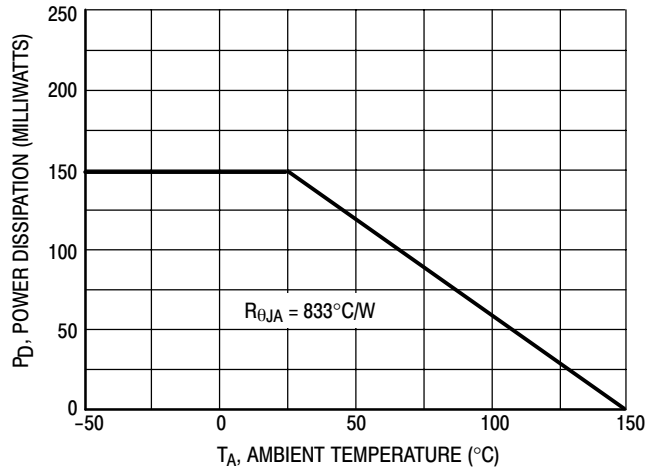


Figure 1. Derating Curve

NSTB1002DXV5T1G, NSTB1002DXV5T5G

TYPICAL ELECTRICAL CHARACTERISTICS — PNP TRANSISTOR

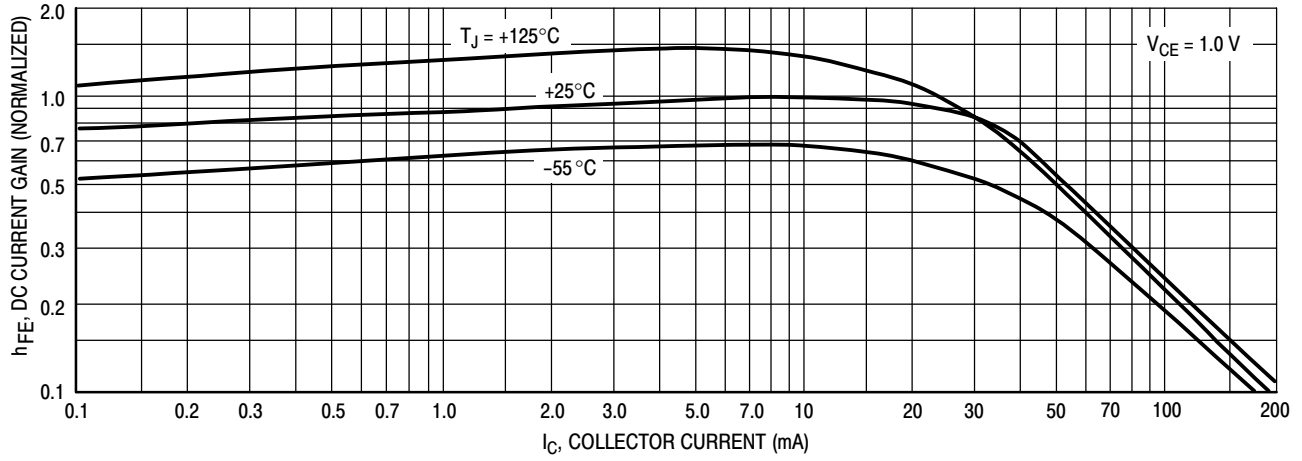


Figure 2. DC Current Gain

NSTB1002DXV5T1G, NSTB1002DXV5T5G

TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

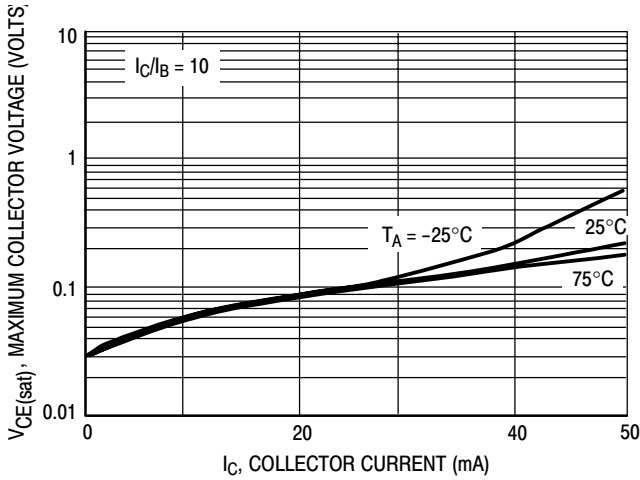


Figure 3. $V_{CE(sat)}$ versus I_C

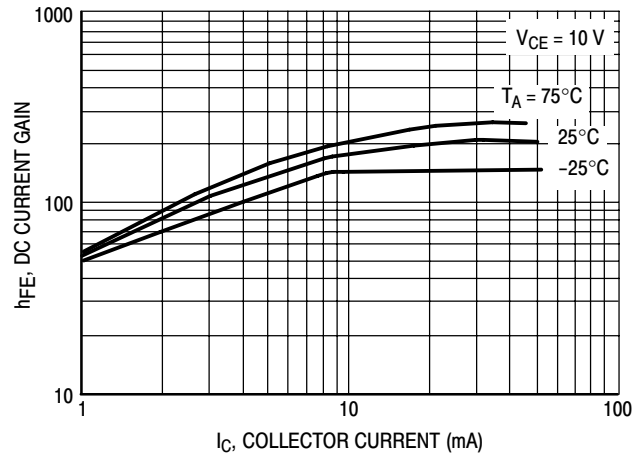


Figure 4. DC Current Gain

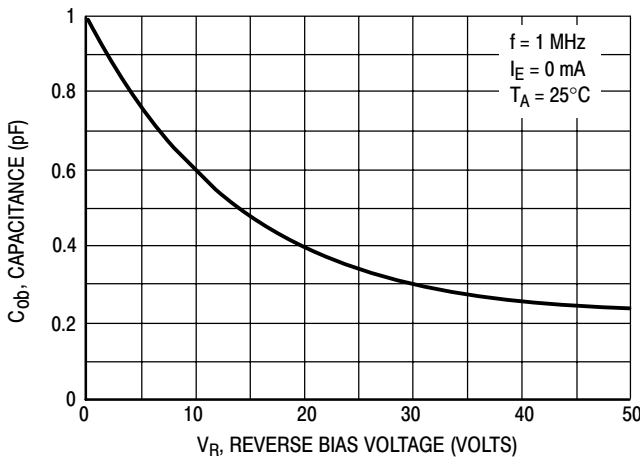


Figure 5. Output Capacitance

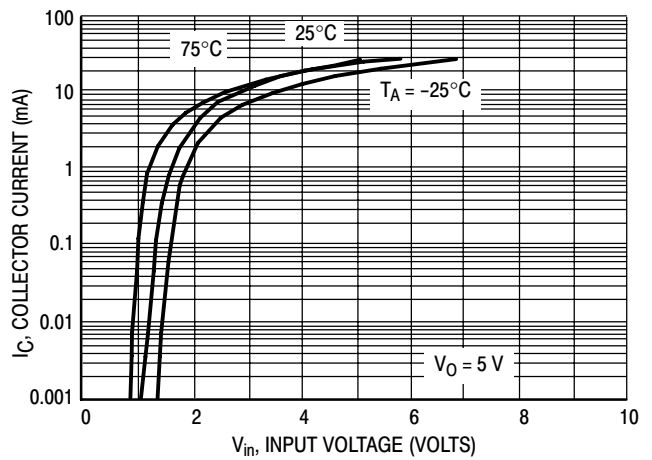


Figure 6. Output Current versus Input Voltage

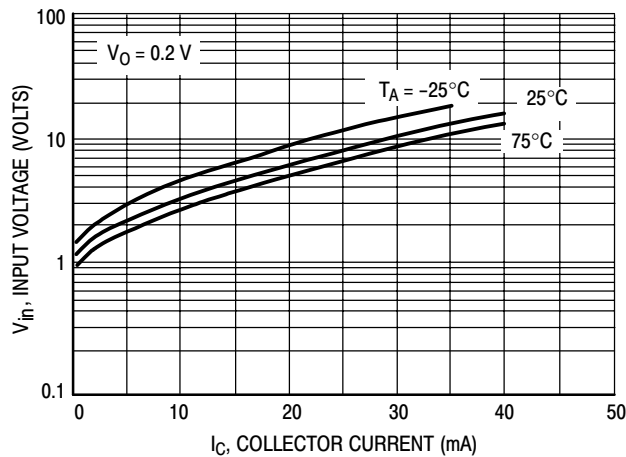
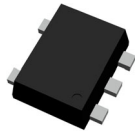


Figure 7. Input Voltage versus Output Current

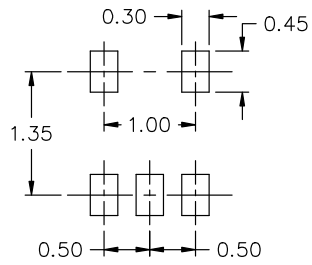
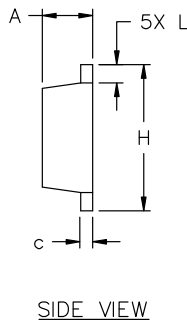
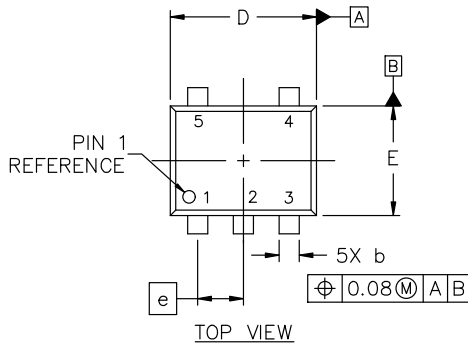
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-553-5 1.60x1.20x0.55, 0.50P
CASE 463B
ISSUE D

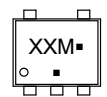
DATE 21 FEB 2024



- NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
 2. ALL DIMENSIONS ARE IN MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.55 | 1.60 | 1.65 |
| E | 1.15 | 1.20 | 1.25 |
| e | 0.50 BSC | | |
| H | 1.55 | 1.60 | 1.65 |
| L | 0.10 | 0.20 | 0.30 |

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT*
 * FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- | | | | | |
|---|--|---|---|--|
| <p>STYLE 1: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR</p> | <p>STYLE 2: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4</p> | <p>STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1</p> | <p>STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2</p> | <p>STYLE 5: PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE</p> |
| <p>STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 1 5. COLLECTOR 2/BASE 1</p> | <p>STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR</p> | <p>STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER</p> | <p>STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE</p> | |

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| DESCRIPTION: | SOT-553-5 1.60x1.20x0.55, 0.50P | PAGE 1 OF 1 |

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