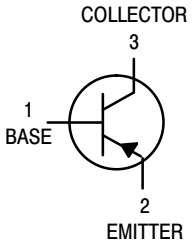
PNP General Purpose Transistor

NST3906F3T5G

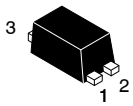
The NST3906F3T5G device is a spin−off of our popular SOT−23/SOT−323/SOT−563/SOT−963 three−leaded device. It is designed for general purpose amplifier applications and is housed in the SOT−1123 surface mount package. This device is ideal for low−power surface mount applications where board space is at a premium.

Features

- h_{FE}, 100−300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Reduces Board Space
- This is a Pb−Free Device

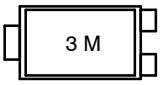


NST3906F3T5G



SOT−1123
CASE 524AA
STYLE 1

MARKING DIAGRAM



3 = Device Code
M = Date Code

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	−40	Vdc
Collector − Base Voltage	V_{CBO}	−40	Vdc
Emitter − Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−200	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D (Note 1)	290 2.3	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	432	°C/W
Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D (Note 2)	347 2.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	360	°C/W
Thermal Resistance, Junction−to−Lead 3	$R_{\Psi JL}$ (Note 2)	143	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 100 mm^2 1 oz, copper traces.
2. 500 mm^2 1 oz, copper traces.

ORDERING INFORMATION

Device	Package	Shipping†
NST3906F3T5G	SOT−1123 (Pb−Free)	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (Note 3) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−40	–	Vdc
Collector – Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	−40	–	Vdc
Emitter – Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 3.0 Vdc)	I_{CEX}	–	−50	nAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = −0.1 mAdc, V_{CE} = −1.0 Vdc) (I_C = −1.0 mAdc, V_{CE} = −1.0 Vdc) (I_C = −10 mAdc, V_{CE} = −1.0 Vdc) (I_C = −50 mAdc, V_{CE} = −1.0 Vdc) (I_C = −100 mAdc, V_{CE} = −1.0 Vdc)	h_{FE}	 60 80 100 60 30	 – – 300 – –	–
Collector – Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc) (I_C = −50 mAdc, I_B = −5.0 mAdc)	$V_{CE(sat)}$	 – –	 −0.25 −0.4	Vdc
Base – Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc) (I_C = −50 mAdc, I_B = −5.0 mAdc)	$V_{BE(sat)}$	 −0.65 –	 −0.85 −0.95	Vdc
SMALL– SIGNAL CHARACTERISTICS				
Current – Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	250	–	MHz
Output Capacitance (V_{CB} = −5.0 V, I_E = 0 mA, f = 1.0 MHz)	C_{obo}	–	4.5	pF
Input Capacitance (V_{EB} = −0.5 V, I_E = 0 mA, f = 1.0 MHz)	C_{ibo}	–	10.0	pF
Noise Figure (V_{CE} = −5.0 Vdc, I_C = −100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	4.0	dB
SWITCHING CHARACTERISTICS				
Delay Time	(V_{CC} = −3.0 Vdc, V_{BE} = 0.5 Vdc)	t_d	–	35	ns
Rise Time	(I_C = −10 mAdc, I_{B1} = −1.0 mAdc)	t_r	–	35	
Storage Time	(V_{CC} = −3.0 Vdc, I_C = −10 mAdc)	t_s	–	250	ns
Fall Time	(I_{B1} = I_{B2} = −1.0 mAdc)	t_f	–	50	

3. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

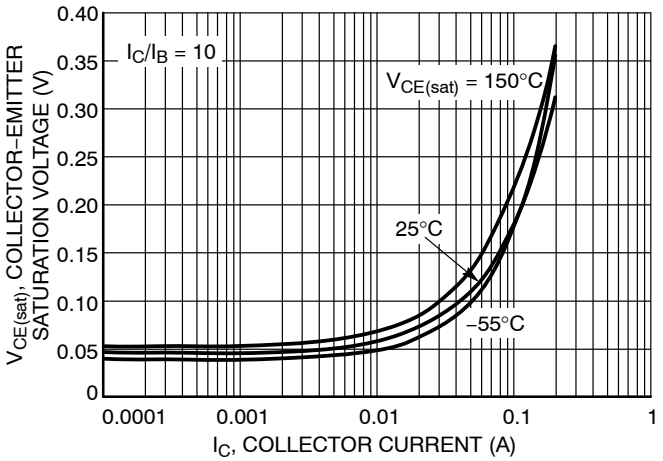


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

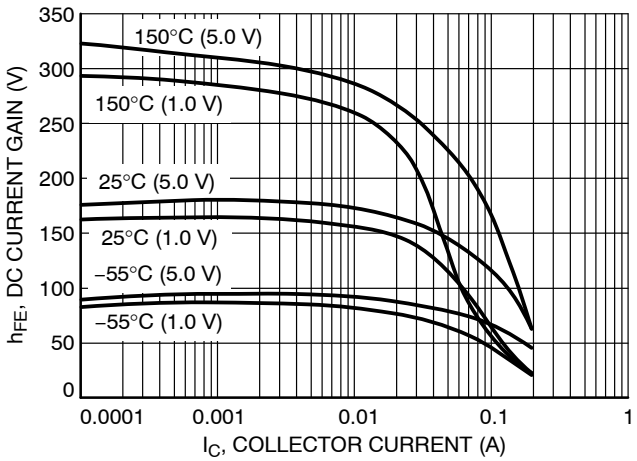


Figure 2. DC Current Gain vs. Collector Current

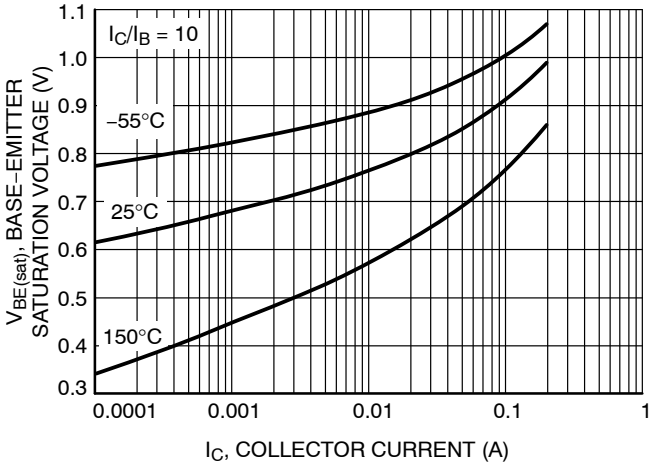


Figure 3. Base Emitter Saturation Voltage vs. Collector Current

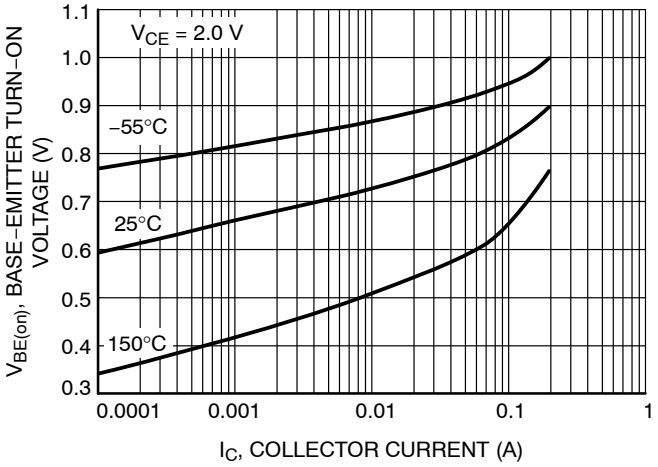


Figure 4. Base Emitter Turn−On Voltage vs. Collector Current

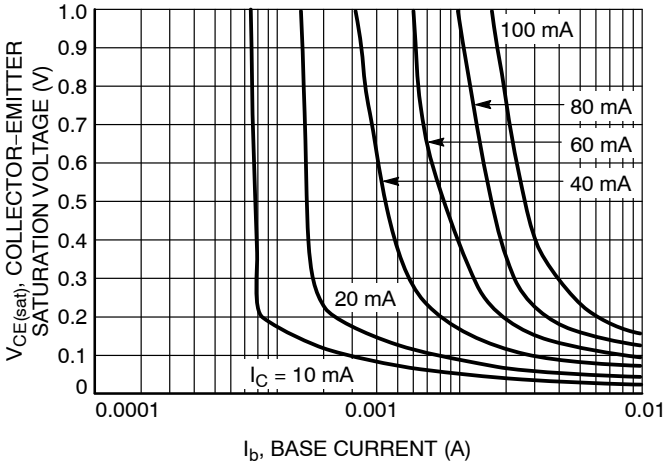


Figure 5. Saturation Region

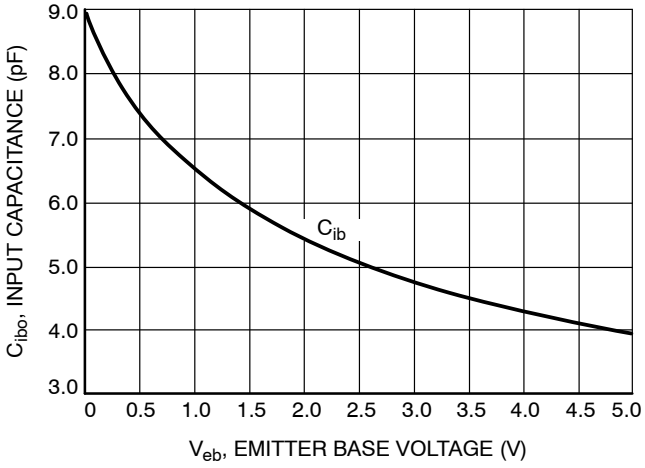


Figure 6. Input Capacitance

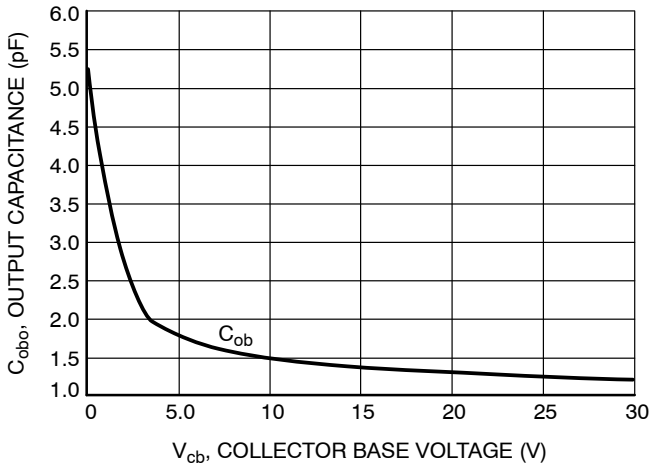
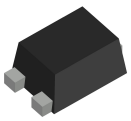
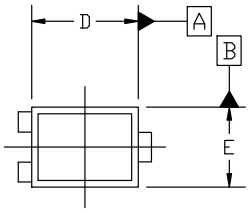


Figure 7. Output Capacitance

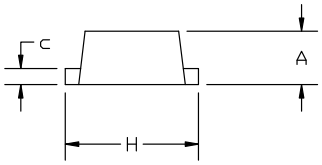


SOT−1123 0.80x0.60x0.37, 0.35P
CASE 524AA
ISSUE D

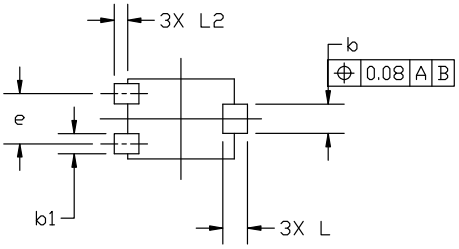
DATE 18 JAN 2024



TOP VIEW



SIDE VIEW



BOTTOM VIEW

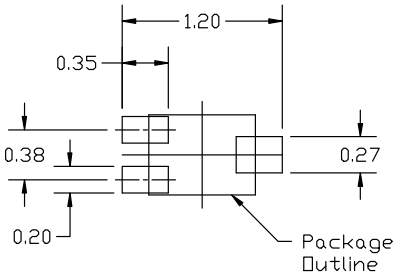
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.15	0.22	0.28
b1	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
e	0.35	0.38	0.40
H	0.950	1.000	1.050
L	0.185 REF		
L2	0.05	0.10	0.15

GENERIC MARKING DIAGRAM*

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

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DESCRIPTION:	**SOT−1123 0.80x0.60x0.37, 0.35P**		**PAGE 1 OF 1**

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